B. Tech with

HONORS

in

VLSI

Academic Regulations, Course Structure and Syllabus

Effective from 2023-24 admitted batches

Offered by

Department of Electronics and Communication Engineering

KSRM College of Engineering (A) – Kadapa

(Approved by AICTE, Accredited by NAAC with A+ Grade and NBA and Affiliated to JNTUA, Anantapuramu)

ELIGIBILITY / REGISTRATION / AWARD OF HONORS

The objective of introducing B.Tech. (Hons.) is to facilitate the students to choose additionally the specialized courses of their choice and build their competence in a specialized area in the UG level. The program is a best choice for academically excellent students having good academic record and interest towards higher studies and research.

i) Honors is introduced in the curriculum of all B. Tech. programs offering a major degree and is applicable to all B.Tech (Regular and Lateral Entry) students admitted in Engineering & Technology.

ii) Those students with **at least 7.0 CGPA without any course backlogs up to III Semester in the major degree are only eligible to register for Honor degree**.

iii) A student shall earn **additional 18 credits for award of Honors** from same branch / department / discipline registered for major degree. This is in addition to 163 credits by a regular student and 123 Credits by a Lateral Entry student for the award of Major degree.

iv) A student is permitted to register for Honors in IV Semester after the results of III Semester are declared. Students shall register and pass in all the courses prescribed and being offered from V semester under the respective Honor degree.

v) Students have to attend classwork for courses under Honor degree beyond regular academic hours meant for major degree. Students can also undergo the courses under Honor through any proctored online platforms with the prior approval of the BoS Chairman and the HoD of the respective department offering Honor degree.

vi) The attendance for the registered courses under Honors and regular courses offered for Major degree in a Semester will be considered separately.

vii) A student shall have an aggregate of 75% attendance in all courses registered under Honors in that particular semester to become eligible for attending Semester-End examinations.

viii) The registration for the Honor will be cancelled, if the student is detained due to lack of attendance in Major,

ix) The registration for the Honor will be cancelled, if the student fails in any course of either Honor / Major in any semester from V to VIII Semester.

x) A student registered for Honors shall pass in all subjects that constitute the requirement for the Honors degree program. No class/division (i.e., second class, first class and distinction, etc.) will be awarded for Honors degree program.

xi) A separate grade sheet will be issued for the Honor degree courses semester-wise.

xii) If a student drops or is terminated from the Honors program, the additional credits so far earned cannot be converted into open or core electives; they will remain extra.

xiii) The Honors will be mentioned in the degree certificate as Bachelor of Technology (Honors) in XYZ. For example, B.Tech. (Honors) in Mechanical

Engineering.

xiv) There shall be a minimum enrolment of 20% OR 20 enrollments from the list of eligible students to offer Honors program.

xv) There is no fee for registration of courses for Honors program offered.

xvi) A student can register for either Minor / Honor but not both.

xvii) Student shall submit an application for either Minor / Honor at least one week before the commencement of the V Semester.

HONORS PROGRAMS OFFERED

Offering Department	Title	Who can Register
Civil Engineering	Civil Engineering	B.Tech. CE
	Tunnel Engineering	
	Interior Design	
Mechanical Engineering	Mechanical Engineering	B.Tech. ME
Electrical and Electronics Engineering	Electric Vehicles	B.Tech. EEE
Electronics and Communication Engineering	VLSI	B.Tech. ECE
	Embedded Systems and IoT	
Computer Science and Engineering	Computer Science and Engineering	B.Tech. CSE, B.Tech. AIML, B.Tech. CSE(DS), B.Tech. CSE(AIML)
	Artificial Intelligence and Machine Learning	
	Data Science	
	CSE-Artificial Intelligence and Machine Learning	

COURSE STRUCTURE

for

HONORS

in

VLSI

S. No	COURSE CODE	COURSE TITLE	Semester Offered	L	T	P	IM	EM	CR
1	2304571H	Analog IC Design	V	3	0	0	30	70	3
2	2304572H	Digital IC Design	V	3	0	0	30	70	3
3	2304671H	Digital Design Through System Verilog	VI	3	0	0	30	70	3
4	2304672H	VLSI Design Flow: RTL to GDS	VI	3	0	0	30	70	3
5	2304771H	CPLD & FPGA Architectures and Applications	VII	3	0	0	30	70	3
6	2304772H	Applied Project Work	VII	0	0	6	60	140	3
			Total	**15**	**0**	**6**	**210**	**490**	**18**

2304571H	HONORS IN VLSI ANALOG IC DESIGN (ECE)	L	T	P	C
		3	0	0	3

Pre-Requisites: Nil

Course Outcomes:

On successful completion of the course, student will be able to

CO1. Understand the MOSFET characteristics, biasing techniques and current mirrors for analog circuit design.

CO2. Analyse single-stage amplifiers and their performance with feedback and cascode configurations.

CO3. Design and analyze the performance of differential amplifiers in analog circuits.

CO4. Learn the characteristics and compensation techniques of operational amplifiers.

CO5. Understand the design principles of bandgap reference circuits.

SYLLABUS

UNIT - I: REVIEW OF MOSFET DEVICE CHARACTERISTICS (10 Periods)

Second order effects, MOS small signal Model, Capacitances, body bias effect, Current biasing, voltage biasing, Technology biasing, Relative comparison and limitations. Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks.

Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Wilder current mirrors, voltage and current references, Mismatch in accuracies, Design solutions to minimize is match in accuracies.

UNIT - II: SINGLE-STAGE AMPLIFIERS (10 Periods)

Analytical justification of operating region suitable for amplification/switching. Design of CS amplifier with different loads, Limitations of diode connected load, Improving output impedance of CS amplifier through feedback, small signal analyses of common gate and common drain topologies and their frequency response with parasitic affects, significance of cascode, design of cascode amplifier and with ideal current source load and practical cascode load, Limitations of cascode, folded cascode amplifier and design with parasitics.

UNIT - III: DIFFERENTIAL AMPLIFIERS AND CURRENT MIRRORS (09 Periods)

Significance of differential signaling, Limitations of quasi differential amplifier, Design of differential amplifier with current source load and diode connected load and small signal analyses, errors due to mismatch, replication principle, qualitative analysis, common mode response, gilbert cell, Common centroid layout.

UNIT - IV: OPERATIONAL AMPLIFIER (08 Periods)

Characterization, two stage Op-amp, small signal analysis, Miller compensation, effect of RHP zero on stability, Lead compensation, constant gm biasing, design of biasing circuit independent of process and temperature variations

UNIT-V: BAND GAP REFERENCE (08 Periods)

General considerations, Supply independent biasing, temperature independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, curvature correction, Design of BGR under low voltage conditions

Total Periods: 45

TEXT BOOKS:

T1. Design of analog CMOS Integrated circuit, BehzadRazavi, McGraw-Hill education,2017, Second Edition.
T2. Analysis and Design of Analog Integrated Circuits, Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Wiley, 2024, Sixth edition.
T3. Analog VLSI: Signal and information processing, Mohammed Ismail and Terrifiez, Tata McGraw-Hill, 1994.

REFERENCE BOOKS:

R1. VLSI design techniques for analog and digital Circuits, Randall. Geiger, Phillipe. AllemandNoelr. Strader, Tata McGraw-Hill Education, 1989.
R2. Analog Integrated Circuit Design, David johns, Tony Chan Carusone and Kenneth martin, Wiley, 2011, Second edition.
R3. Systematic Design of Analog CMOS Circuits, Paul G. A. JespersAnd Boris Murmann, Cambridge University Press, 2017.

WEB RESOURCES:

1. https://ocw.mit.edu/courses/6-012-microelectronic-devices-and-circuits-fall-2009/
2. https://nptel.ac.in/courses/117106030
3. https://nptel.ac.in/courses/108106105
4. https://www2.eecs.berkeley.edu/Faculty/Homepages/niknejad.html

2304572H	HONORS IN VLSI DIGITAL IC DESIGN (ECE)	L	T	P	C
		3	0	0	3

Pre-Requisites: Nil

Course Outcomes:

On successful completion of the course, student will be able to

CO1. Understand the basics of MOS Design.
CO2. Design of Combinational MOS Logic Circuits and the basics of Sequential MOS Logic Circuits.
CO3. Analyze concepts of digital integrated circuits and its applications.
CO4. Understand concepts of different interconnection techniques.
CO5. Describe concepts of Semiconductor memories and RAM array Organization.

SYLLABUS

UNIT - I: MOS DESIGN (08 Periods)

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT - II: COMBINATIONAL MOS LOGIC CIRCUITS (11 Periods)

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates, Multipliers.

UNIT - III: SEQUENTIAL MOS LOGIC CIRCUITS (08 Periods)

Behaviour of bi stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT - IV: DYNAMIC LOGIC CIRCUITS (10 Periods)

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits. Interconnect: Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, Advanced Interconnect Techniques, clock distribution networks, clock delays, clock skew and Jitter.

UNIT - V: SEMICONDUCTOR MEMORIES (08 Periods)

Flash Memory, Memory Types, RAM array organization, DRAM – Types, Operation, Leakagecurrents in DRAM cell and refresh operation, SRAM

operation Leakage currents in SRAM cells,Flash Memory-NOR flash and NAND flash.

Total Periods: 45

TEXT BOOKS:

T1. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2nd Ed., PHI.
T2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
T3. Modern VLSI Design-Wayne Wolf, Fourth edition, Copyrights 2009.
T4. Digital Integrated circuits, J. Rabey & B. Nikolic, Second Edition, Pearson, 2003

REFERENCE BOOKS:

R1. CMOS Circuit Design, Layout, and Simulation, R. Jacob Baker, Wiley, 2010, Third Edition.
R2. Digital Integrated Circuits, John M. Rabaey, PHI, EEE, 1997.
R3. CMOS Digital Integrated Circuits - Analysis and Design, Sung-Mo Kang, Yusuf Leblebici, McGraw-Hill, Fourth Edition, 2014.

WEB RESOURCES:

1. https://onlinecourses.nptel.ac.in/noc20_ee05/preview
2. https://ocw.mit.edu/courses/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/pages/lecture-notes/

2304671H	HONORS IN VLSI DIGITAL DESIGN THROUGH SYSTEM VERILOG (ECE)	L	T	P	C
		3	0	0	3

Pre-Requisites: Nil

Course Outcomes:

On successful completion of the course, student will be able to

CO1. Understand the fundamentals of digital logic circuits and the role of System Verilog.
CO2. Apply System Verilog constructs to model digital circuits using modelling styles.
CO3. Analyse digital systems through testbenches for functionality and timing correctness.
CO4. Design modular and parameterized digital systems using System Verilog constructs.
CO5. Evaluate the performance of HDL code for implementation on FPGA/ASIC platforms.

SYLLABUS

UNIT - I: INTRODUCTION TO SYSTEMVERILOG (08 Periods)

Digital system basics: combinational and sequential logic, RTL design flow: simulation, synthesis, verification, Introduction to System Verilog vs Verilog, Design entry, modules, ports, data types, and literals.

UNIT - II: COMBINATIONAL DESIGN WITH SYSTEM VERILOG (07 Periods)

Modelling logic gates, multiplexers, decoders, encoders, Continuous assignments (assign), Procedural blocks: always_comb, always_latch, Case study: ALU design in System Verilog.

UNIT - III: SEQUENTIAL LOGIC DESIGN (10 Periods)

Flip-flops, latches, registers, counters always_ff block, synchronous and asynchronous resets, FSM (Finite State Machine) modelling: Mealy and Moore, FSM case study: traffic light controller.

UNIT-IV: SYSTEM VERILOG CONSTRUCTS AND CODING GUIDELINES (7 Periods)

Blocking vs non-blocking assignments, if, case, for, foreach, unique, priority, typedef, enum, struct, union, Design for synthesis guidelines.

UNIT-V: TIMING, SIMULATION & VERIFICATION, SYNTHESIS
(13 Periods)

Timing analysis, setup/hold time, metastability, Testbench architecture, Basic simulation using ModelSim/other tools, Assertions and simple functional verification (assert, cover), RTL coding for synthesis, Resource sharing, pipelining, clock gating, Synthesis tool introduction (like Synopsys Design Compiler, Xilinx Vivado).

Total Periods: 45

TEXT BOOKS:

T1. Verilog HDL: A Guide to Digital Design and Synthesis, (for Verilog base), Samir Palnitkar,

T2. System Verilog for Design: A Guide to Using System Verilog for Modeling, Simulation, and Synthesis. Stuart Sutherland

REFERENCE BOOKS:

R1. VHDL and System Verilog for Hardware Design. Perry, D.L.

R2. Online tools and simulators: EDA Playground, ModelSim, Vivado, Quartus.

WEB RESOURCES:

1. https://onlinecourses.nptel.ac.in/noc24_cs61/preview
2. https://jrasti.ir/wp-content/uploads/2024/09/designing-digital-systems-systemverilog.pdf

2304672H	HONORS IN VLSI VLSI DESIGN FLOW: RTL TO GDS (ECE)	L	T	P	C
		3	0	0	3

Pre-Requisites: Nil

Course Outcomes:

On successful completion of the course, student will be able to

CO1. Understand the complete ASIC/SoC design flow from RTL to GDSII.
CO2. Analyze RTL design using Verilog and synthesis using industry-standard tools.
CO3. Apply logic synthesis and physical design steps like floor planning, placement, clock tree synthesis, and routing.
CO4. Evaluate design performance using static timing analysis (STA), DRC, LVS checks.
CO5. Implement low-power design and optimization techniques during the VLSI design flow.

SYLLABUS

UNIT - I: INTRODUCTION TO VLSI DESIGN FLOW (08 Periods)

ASIC vs FPGA, Front-end and Back-end design flow, EDA tools overview, RTL to GDS flow overview

UNIT - 2: RTL DESIGN AND SIMULATION (07 Periods)

Verilog HDL design constructs, RTL coding guidelines for synthesis, Functional simulation and testbench, Design constraints (SDC)

UNIT - 3: LOGIC SYNTHESIS (10 Periods)

Technology mapping, Combinational and sequential optimization, Multi-cycle and false path handling, Netlist generation and optimization

UNIT - 4:STATIC TIMING ANALYSIS AND TIMING CLOSURE (10 Periods)

Setup and hold analysis, Timing paths and critical paths, Clock uncertainty, skew, and jitter, Timing reports and fixing violations

UNIT - 5: FLOORPLANNING AND PLACEMENT AND ROUTING (10 Periods)

I/O planning, Macro placement and power planning, Congestion analysis and legalization, Clock Tree Synthesis (CTS), Global and detailed routing, Crosstalk and IR drop analysis, Design Rule Check (DRC) and Layout vs Schematic (LVS), Final GDSII generation and signoff

Total Periods: 45

TEXT BOOKS:

T1. On-Chip Communication Architectures-System on Chip Interconnect, SudeepPasricha&NikilDutt, Morgan Kaufmann Publishers
T2. Digital Integrated Circuits, Jan M. Rabaey, Prentice Hall (1995) Pearson.

REFERENCE BOOKS:

R1. Advanced ASIC chip synthesis using Synopsys Design Compiler, Physical Compiler, and Prime Time, HimanshuBhatnagar - Kluwer Academic publisher (2002)
R2. EDA Tool Manuals – Synopsys, Cadence (User manuals and flow documents).

WEB RESOURCES:

1. https://nptel.ac.in/courses/108106191
2. https://onlinecourses.nptel.ac.in/noc23_ee137/preview
3. https://sites.google.com/site/snehsaurabhhome/teaching/nptel-vlsi-design-flow-rtl-to-gds
4. https://www.cadence.com/en_US/home/training/all-courses/86136.html

2304771H	HONORS IN VLSI CPLD AND FPGA ARCHITECTURES (ECE)	L	T	P	C
		3	0	0	3

Pre-Requisites: Nil

Course Outcomes:

On successful completion of the course, student will be able to

CO1. Differentiate between ROM, PAL, PLA, SPLD, CPLD, FPGA.
CO2. Compare the features of Various CPLDs in terms of their architecture, Logic blocks
CO3. Compare the features of Various FPGAs in terms of their Architecture, Configurable logic block and routing.
CO4. Gain knowledge on routing algorithms adopted in FPGAs.
CO5. Test a particular PLD using various techniques like design validation, Timing verification.

SYLLABUS

UNIT - I: PROGRAMMABLE LOGIC (08 Periods)

Programmable read only memory (PROM), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT - II: FPGAs (10 Periods)

Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT - III: CPLD's (10 Periods)

Complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of Altera flex logic 10000 series CPLD's, max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypress flash 370 device technology, lattice PLSI's architectures.

UNIT - IV: PLACEMENT (10 Periods)

Objectives, placement algorithms: Minute-Based placement, iterative improvement placement, simulated annealing. Routing: objectives, segmented channel routing, Maze routing, Rout ability estimation, Net delays, computing signal delay in RC tree networks. skew and jitter.

UNIT-V: TOOLS FOR FPGAS & ASICS (07 Periods)

Digital Front End and back-End tools for FPGAs & ASICs, FPGA implementation steps Verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, and programmability
failures.

Total Periods: 45

TEXT BOOKS:

T1. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, Pearson Education 2009.

T2. Field Programmable Gate Array Technology, S.Trimberger, Edr, Kluwer Academic Publications, 1994.

T3. Algorithms for VLSI Physical Design Automation, N. A. Sherwani, Boston, MA, USA: Springer, 1999, Third edition.

REFERENCE BOOKS:

R1. Field Programmable Gate Arrays, Old Field, R. Dorf, John Wiley & Sons, New York, 1995.

R2. Field Programmable Gate array Brown, R. Francis, J. Rose, Z. Vransic, KluwerPubln, 1992.

R3. Digital Integrated Circuits: A Design Perspective, J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Upper Saddle River, NJ, USA: Pearson Education, Second Edition,2003.

WEB RESOURCES:

1. https://eee.poriyaan.in/topic/cpld--complex-programmable-logic-devices--11688/
2. Microsoft PowerPoint - ece428_fpgaarch [Compatibility Mode]
3. Class 217: Introduction to CPLD and FPGA Design, Part 1

2302772H	HONORS IN VLSI APPLIED PROJECT WORK (ECE)	L	T	P	C
		0	0	6	3

Pre-Requisites: VLSI Design Flow: RTL to GDS, CPLD & FPGA Architectures and Applications

Course Outcomes:

On successful completion of the course, student will be able to

CO1. Design of digital circuits using CMOS logic structures.
CO2. Apply appropriate tools and simulate the designed circuit.
CO3. Evaluate the performance of the circuit and calculate design metrics.
CO4. Analyze the problems following professional ethics with focus on societal and environmental aspects.
CO5. Work as a team and communicate results in an effective way.
CO6. Make decisions as an individual or as a team member to manage tasks and also engage in independent and life-long learning with ability to adapt to new and technological changes.