KANDULA SRINIVASA REDDY MEMORIAL COLLEGE OF ENGINEERING
(AUTONOMOUS)

KADAPA-516003. AP

(Approved by AICTE, Affiliated to JNTUA, Ananthapuramu, Accredited by NAAC)

(An ISO 9001-2008 Certified Institution)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VALUE ADDED COURSE

ON

"DESIGN OF VLSI SUBSYSTEMS"

Resource Person : Dr. M Madhusudhan Reddy, Associate Professor, Dept. of ECE, KSRMCE

Resource Person : Smt. K. Divya Lakshmi, Assistant Professor, Dept. of ECE, KSRMCE

Course Coordinator: Dr. M Madhusudhan Reddy, Associate Professor, Dept. of ECE, KSRMCE

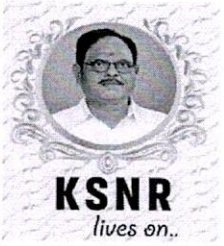
Course Coordinator: P. Subbarayudu, Assistant Professor, Dept. of ECE, KSRMCE

Duration: 01/05/2024 to 22/06/2024

K.S.R.M. COLLEGE OF ENGINEERING
(UGC-AUTONOMOUS)
Kadapa, Andhra Pradesh, India– 516 005

Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

An ISO 14001:2004 & 9001: 2015 Certified Institution



Lr./KSRMCE/ECE/2023-24/ Date:25-04-2024

To
The Principal,
KSRMCE,
Kadapa.

Respected Sir,

Sub: Permission to Conduct Value added Course on "Design of VLSI Subsystems" **01/05/2024 to 22/06/2024**–Req- Reg.

The Department of Electronics and Communication Engineering is planning to offer a Value-Added Course on "Design of VLSI Subsystems" to VI Sem ECE B.Tech. students. The course will be conducted from **01/05/2024 to 22/06/2024**. In this regard, I kindly request you to grant permission to conduct Value Added Course.

Thanking you sir,

Forwarded to the Principal Sir

Yours faithfully

(Dr.M.MadhusudhanReddy,
Assoc.Professor in ECED)

Permitted
V.S.S. Murty
25/04/2024

K.S.R.M. COLLEGE OF ENGINEERING

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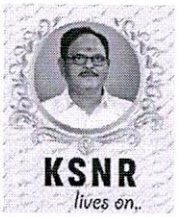

Cr./KSRMCE/ECE/2023-24/

Date: 27-04-2024

Circular

The Department of Electronics & Communication Engineering is offering a Value Added Course on "Design of VLSI Subsystems" from **01/05/2024 to 22/06/2024** to VI Sem ECE B.Tech students. In this regard, interested students are requested to register their names for the Value Added Course with Course Coordinator.

For further information contact Course Coordinator.

Course Coordinator: Sri. P. Subbarayudu, Assist. professor, Dept. of ECE. KSRMCE.
Contact No : 7013375604

HOD

Dept. of ECE

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 005

Cc to:

IQAC-KSRMCE

K.S.R.M. COLLEGE OF ENGINEERING

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Kadapa, Andhra Pradesh, India– 516 005

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Date:29/04/24

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REGISTRATION FORM

Value Added Course

On

"Design of VLSI Subsystems" From 01/05/2024 to 22/06/2024

S.No	Full Name	Roll Number	Branch	Semester	Signature
1	V. Bhanu Venkata Prakash	229Y5A0422	ECE	VI	V.B.K Prakash
2	A. Bhanu prakash	219Y1A0407	ECE	VI	A. Bhanu
3	D. Naga lakshmi	219Y1A0443	ECE	VI	D. Naga
4	D. Rathna Srija	219Y1A0485	ECE	VI	D. Rathna
5	P. Manideep Reddy	219Y1A0467	ECE	VI	P. Manideep
6	G. Anjitha	229Y5A0407	ECE	VI	G. Anjitha
7	G. Saikonda Reddy	219Y1A0444	ECE	VI	G. Saikonda
8	C. Ajaykumar.	219Y1A0432	ECE	VI	C. Ajay
9	C. Kishore kumar	219Y1A0424	ECE	VI	C. Kishore
10	N. Divakar	219Y1A0486	ECE	VI	N. Divakar
11	K. Mallesh	219Y1A0483	ECE	VI	K. Mallesh
12	M. Divakar Reddy	219Y1A0499	ECE	VI	M. Divakar
13	T. Bhargavi	219Y1A0459	ECE	VI	T. Bhargavi
14	T. Sindhu	229Y5A0418	ECE	VI	T. Sindhu
15	B. Karthik Reddy	219Y1A0413	ECE	VI	B. Karthik
16	K. Sindhu priya	219Y1A0481	ECE	VI	K. Sindhu priya
17	K. Sai Narasimha.	219Y1A0465	ECE	VI	K. Sai Narasimha
18	T. Manikanta	229Y5A0419	ECE	VI	T. Manikanta
19	M. Obulamma	219Y1A0496	ECE	VI	M. Obulamma
20	K. R. Priyanjali	219Y1A0469	ECE	VI	K. R. Priyanjali
21	B. poornima	219Y1A0408	ECE	VI	B. poornima
22	p. chandana	219Y1A0466	ECE	VI	P. Chandana

23	K. Praveen	219Y1A0479	ECE	VI	K. Praveen.
24	C.V.Vasanth Reddy	219Y1A0491	ECE	VI	C.Vasanth
25	C. Renuka	219Y1A0427	ECE	VI	C. Renuka
26	G. Ganesh	219Y1A0419	ECE	VI	G
27	B.Chinni Krishna	219Y1A0418	ECE	VI	B.Chinni Krishna
28	C.Pavan kalyan..	219Y1A0423	ECE	VI	CPK
29	N.HanumanthReddy	219Y1A04A8	ECE	VI	Hanumanth
30	N.VishnuvardhanReddy	219Y1A04B6	ECE	VI	N.Vishnu
31	G.venkata krishna	219Y1A0450	ECE	VI	G.V.Krishna
32	C.Ravikumar	219Y1A0428	ECE	VI	C.Ravikumar
33	M. Sai Ram Naik	219Y1A04A6	ECE	VI	M. Sai Ram Naik
34	~~B. Harshitha~~	~~219Y1A04H9~~	~~ECE~~	VI	~~Harshitha~~
35	S. Rahiman	219Y1A04E3	ECE	VI	S. Rahiman
36	P. Devendra	219Y1A04D0	ECE	VI	P. Devendra
37	G. Prem Kumar	219Y1A0446	E.C.E	VI	G. Prem Kumar
38	O. Naveen Kumar	219Y1A0460	ECE	VI	O. Naveen Kumar
39	S. Srikanth	219Y1A04F7	ECE	VI	S. Srikanth
40	C. Kiran kumar	219Y1A0426	ECE	VI	C. Kiran kumar
41	C.V. Akhil	219Y1A0433	ECE	VI	C.V. Akhil
42	S. Manasa	219Y1A04F4	ECE	VI	S. Manasa
43	N. Divakar	219Y1A04B0	ECE	VI	Divakar
44	B. Karthik Reddy	219Y1A0413	ECE	VI	Karthik
45	K. Harikrishna Reddy	219Y1A0461	ECE	VI	Harikrishna
46	M. Mallikarjuna	219Y1A0495	ECE	VI	Mallikarjuna
47	P. Vijaya Simhaprasad	219Y1A04C2	ECE	VI	Vijaya Simhaprasad
48	P. Satya Narayana	219Y1A04C5	ECE	VI	Satya Narayana
49	S. V. Nikhil varma	219Y1A0461	ECE	VI	S.V. Nikhil varma
50	S. Srinath	219Y1A04F3	ECE	VI	Srinath
51	S. Srikanth	219Y1A04F7	ECE	VI	Srikanth

1. M. Reddy
2.

Coordinator

HOD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

Syllabus of Value Added Course

Course Name: Design of VLSI Subsystems

Course Objectives:

1. The course focuses more on power estimation, and interconnect aware designs
2. Discusses on few power benefits designs.
3. Approximate computing datapath subsystem designs will be analyzed along with the design, and error metrics.

Course Outcomes:

1. Understand the basic Physics and Modelling of MOSFETs.
2. Learn the basics of Fabrication and Layout of CMOS Integrated Circuits.
3. Study & analyze the performance of CMOS Inverter circuits based on their operation, working.
4. Study the Static CMOS Logic Elements.
5. Study the Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families.

UNIT-I CMOS Transistors and Current model, CMOS Inverter and characteristics

Understanding Silicon, Introduction to NMOS, NMOS Transistor Working, PMOS Transistor, MOS Capacitances, Channel Length modulation index, DC characteristics of Inverter, Transfer characteristics of Inverter, Skewed Inverter, Skewed Inverter and threshold voltage

UNIT-II Noise Margin and Delay of Inverter & RC Delay

Noise margin characteristics of inverter, Noise margin parameters, Introduction to Delay in CMOS, Transient analysis of CMOS Inverter, RC approximated delay, Switching Resistance, CMOS Inverter approximated to RC Circuit, Elmore delay, Delay of FO4 inverter, Extracting capacitances of 3-Nand gate for delay estimation, Characterizing Delay of NOR gate

UNIT-III Delay optimization & Combinational Circuit Family

Logical effort and Parasitic delay for different gates, Optimizing Gate Size, Optimizing Gate Sizes Example, Introduction to Combinational Circuit and assymetric gates, Assymetric Gates analysis, Assymetric Gates analysis using short-channel current model, Introduction to Skewed

gates, Skewed gates and best P/N ratio, Introduction to Pseudo NMOS, Psudeo NMOS gates, Dynamic Logic and Domino logic

UNIT-IV Stick Diagram & Power

Introduction to Stick Diagram, Stick Diagram for different gates, Applying Eulers path for stick diagram representations, Multiplexer design and layout, Switching Power and Energy Estimation, Activity factor and estimating dynamic power for a combinational circuit design, Analyzing Dynamic Power

UNIT-V CMOS flip-flop, Adder subsystem design

CMOS Latch and flipflop design.,1-bit Adder design, Adder-Part2, PG architecture - Part1, PG architecture - Part2, Carry Skip Adder, Carry Look Ahead and Carry Increment Adder, Approximate Multipliers - Part 1, Approximate Multipliers - Part 2

Text Books/Reference Books:

1.N. Weste and D. Harris, CMOS VLSI Design A Circuits and Systems Perspective, 4th edition, Pearson.

2.J M Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits A Design Perspective.

Professor & H.O.D.
Department of E.C.E.
S.R.M. [illegible] Engineering
[illegible]

SCHEDULE

Department of ELECTRONICS AND COMMUNICATION ENGINEERING

Value Added Course

On

"DESIGN OF VLSI SUBSYSTEMS" From 01/05/2024 to 22/06/2024

Date	Timing	Resource Person	Topic to be covered
1/5/24	3 PM to 5 PM	M Madhusudhan Reddy	Understanding Silicon, Introduction to NMOS, NMOS Transistor Working, PMOS Transistor
2/5/24	3 PM to 5 PM	K. Divya Lakshmi	MOS Capacitances, Channel Length modulation index
3/5/24	3 PM to 5 PM	K. Divya Lakshmi	Skewed Inverter, Skewed Inverter and threshold voltage
4/5/24	3 PM to 5 PM	K. Divya Lakshmi	DC characteristics of Inverter, Transfer characteristics of Inverter
6/5/24	3 PM to 5 PM	M Madhusudhan Reddy	Noise margin characteristics of inverter, Noise margin parameters
7/5/24	3 PM to 5 PM	M Madhusudhan Reddy	Introduction to Delay in CMOS, Transient analysis of CMOS Inverter
8/5/24	3 PM to 5 PM	M Madhusudhan Reddy	RC approximated delay, Switching Resistance, CMOS Inverter approximated to RC Circuit
9/5/24	3 PM to 5 PM	M Madhusudhan Reddy	Elmore delay, Delay of FO4 inverter
10/5/24	3 PM to 5 PM	M Madhusudhan Reddy	Extracting capacitances of 3-Nand gate for delay estimation, Characterizing Delay of NOR gate
5/6/24	3 PM to 5 PM	M Madhusudhan Reddy	Logical effort and Parasitic delay for different gates, Optimizing Gate Size, Optimizing Gate Sizes Example
6/6/24	3 PM to 5 PM	M Madhusudhan Reddy	Introduction to Combinational Circuit and assymetric gates, Assymetric Gates analysis, Assymetric Gates analysis using short-channel current model
7/6/24	3 PM to 5 PM	M Madhusudhan Reddy	Introduction to Skewed gates, Skewed gates

			and best P/N ratio
10/6/24	3 PM to 5 PM	K. Divya Lakshmi	Introduction to Pseudo NMOS, Psudeo NMOS gates, Dynamic Logic and Domino logic
11/6/24	3 PM to 5 PM	M Madhusudhan Reddy	Introduction to Stick Diagram, Stick Diagram for different gates
12/6/24	3 PM to 5 PM	K. Divya Lakshmi	Applying Eulers path for stick diagram representations, Multiplexer design and layout
13/6/24	3 PM to 5 PM	K. Divya Lakshmi	Switching Power and Energy Estimation, Activity factor and estimating dynamic power for a combinational circuit design, Analyzing Dynamic Power
14/6/24	3 PM to 5 PM	M Madhusudhan Reddy	CMOS Latch and flipflop design
15/6/24	3 PM to 5 PM	K. Divya Lakshmi	1-bit Adder design, Adder-Part2, PG architecture - Part1, PG architecture - Part2
18/6/24	3 PM to 5 PM	K. Divya Lakshmi	Carry Skip Adder, Carry Look Ahead and Carry Increment Adder
19/6/24	3 PM to 5 PM	M Madhusudhan Reddy	Approximate Multipliers - Part 1, Approximate Multipliers - Part 2

1. M Reddy
2. Divya

Resource Person(s)

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Attendance sheet of Value Added Course on "Design of VLSI Subsystems" From 01/05/2024 to 22/06/2024

S. NO	Roll No.	Name of the student	1/5	2/5	3/5	4/5	6/5	7/5	8/5	9/5	10/5	5/6	6/6	7/6	10/6	11/6	12/6	13/6	14/6	15/6	18/6	19/6	20/6	21/6
			2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44
1	219Y1A0407	A Bhanu Prakash	A	2	4	6	A	8	10	12	14	A	16	18	20	22	A	A	24	26	28	A	30	32
2	219Y1A0408	B Poornima	2	4	A	A	A	6	8	10	A	12	14	A	16	18	20	22	A	24	26	28	30	A
3	219Y1A0413	B Karthik Reddy	A	2	4	6	8	10	12	14	A	16	18	20	22	24	A	26	28	30	32	34	36	38
4	219Y1A0418	B Chinni Krishna	A	2	4	A	A	A	6	8	10	12	14	16	A	18	20	22	A	24	A	26	28	30
5	219Y1A0421	C Vasanth Kumar Reddy	2	4	A	A	6	8	10	A	12	14	A	16	18	20	A	22	24	A	26	28	A	30
6	219Y1A0423	C Pavan Kalyan	A	2	4	6	8	10	12	14	16	A	18	20	22	24	26	28	30	32	34	36	38	40
7	219Y1A0426	C Kiran Kumar	2	4	6	A	8	10	12	14	16	18	A	20	22	24	A	26	28	A	A	30	32	34
8	219Y1A0427	C Renuka	A	2	4	A	6	8	A	A	10	12	14	A	16	18	20	A	A	22	24	26	28	30
9	219Y1A0428	C Ravikumar	2	4	A	6	8	10	12	14	A	16	18	20	A	A	22	24	26	28	30	32	34	36
10	219Y1A0429	C Kishore Kumar	2	A	4	6	8	10	A	A	12	14	16	18	20	22	A	24	A	26	28	30	32	34
11	219Y1A0432	C Ajay Kumar	A	2	4	6	A	A	8	10	12	14	A	A	16	18	20	22	24	26	28	30	32	34

12	219Y1A0433	C Usuvandla Akhil	2 4 A 6 8 10 A A 12 14 16 A 18 20 22 24 26 A 28 A 30 32
13	219Y1A0435	D Srija	A 2 4 6 8 A 10 12 14 16 18 20 22 A A 24 26 28 30 32 34 36
14	219Y1A0443	D Naga Lakshmi	2 4 6 8 10 12 A 14 16 18 A 20 22 24 26 28 30 A 32 34 A 36
15	219Y1A0444	G Sai Konda Reddy	A A 2 4 6 8 10 A 12 14 16 A 18 20 22 A 24 26 28 30 32 34
16	219Y1A0446	G Prem Kumar	2 4 6 A 8 A 10 12 14 16 18 20 22 A 24 26 28 30 A 32 34 36
17	219Y1A0449	G Ganesh	A 2 4 6 8 10 A 12 14 A 16 18 A 20 22 A A A 24 26 28 30
18	219Y1A0450	G Venkata Krishna	2 4 A 6 8 A A 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
19	219Y1A0461	K Hari Krishna Reddy	A 2 4 6 8 10 12 14 16 18 20 A 22 24 26 28 30 32 34 36 38 40
20	219Y1A0465	K Sai Narasimha	2 4 6 8 10 A 12 14 16 A 18 20 22 24 A 26 28 30 32 34 36 38
21	219Y1A0469	K Radha Priyanjali	A A 2 4 6 A 8 10 12 A 14 16 18 20 A 22 24 A 26 28 30 32
22	219Y1A0479	Kunduru Praveen	2 A 4 6 8 10 A 12 14 16 18 A A A A A 20 22 24 26 28 30
23	219Y1A0481	K Sindhu Priya	A 2 4 6 8 10 A 12 14 16 A 18 20 22 24 26 28 30 32 34 36 38
24	219Y1A0483	K Mallesh	2 4 6 8 A 10 12 14 A 16 18 90 A 22 A 24 26 28 30 32 34 36
25	219Y1A0496	M Obulamma	A 2 4 6 8 A 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40
26	219Y1A0495	M. Mallikarjuna	2 4 A 6 8 10 12 A 14 16 A 18 20 22 24 26 A 28 30 A 32 34
27	219Y1A0499	M Diwakar Reddy	A 2 4 6 8 A 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 A
28	219Y1A04A0	M Sai Ram Naik	2 4 A 6 8 10 12 A 14 16 18 20 A A A 22 24 26 28 A A 30
29	219Y1A04A8	N Gari Hanumanth Reddy	A 2 4 6 8 10 12 14 A 16 A 18 20 22 24 26 A A 28 30 32 34

46	229Y5A0407	G Anjitha	2	4	6	8	A	10	12	14	16	A	18	A	20	22	A	24	A	26	28	A	30	32		
47	229Y5A0418	T Sindhu	2	4	A	A	6	A	8	10	12	14	A	16	18	A	20	22	24	A	26	28	30	32		
48	229Y5A0419	T Manikanta	A	2	4	A	A	6	8	A	10	12	A	14	16	18	A	20	22	24	A	26	28	30			
49	229Y5A0420	T Anil Kumar	2	4	A	6	8	10	A	12	14	16	18	A	20	22	24	A	26	A	28	30	32	34		
50	229Y5A0422	V Bhanu Venkata Prakash	2	A	4	6	8	A	10	12	A	14	16	18	A	20	22	24	26	A	28	30	A	32		
51	229Y5A0423	S Ganga Harish	2	4	6	A	8	10	12	A	14	16	18	20	22	24	A	26	28	30	A	A	32	34		

Coordinator(s)

HOD

Professor & H.O.D.
Department of E.C.E.
R.G.M.C.E. College of Engg.
NANDYAL - 518 002

30	219Y1A04B0	N Divakar	2 A 4 6 A 8 10 12 14 A 16 A 18 A 20 22 A 24 26 28 30 32
31	219Y1A04B6	N Vishnuvardhan Reddy	2 A A A 4 6 8 10 A 12 14 A A A 16 18 20 A 22 24 26 28
32	219Y1A04C0	O Naveen Kumar	A A 2 4 6 A 8 A 10 12 A 14 16 18 20 A A 22 24 26 28 30
33	219Y1A04C2	P Vijaya Shimha Prasad	2 A 4 6 A 8 A 10 12 A A A 14 16 18 20 22 24 26 28 30 32
34	219Y1A04C5	P Satya Narayana Reddy	A 2 4 6 8 10 12 A A A A A 14 16 18 20 22 A 24 26 A 28
35	219Y1A04C6	P Chandana (W)	2 4 A 6 8 10 12 14 16 18 20 22 A 24 26 28 30 32 34 36 38 40
36	219Y1A04C7	P Manideep Reddy	A 2 4 6 8 10 12 A 14 16 18 20 22 24 26 A 28 30 32 34 36 38
37	219Y1A04D0	P Devendra	2 4 A A A 6 8 A 10 A 12 14 A 16 18 20 A 22 24 26 28 30
38	219Y1A04E1	S Venkata Nikhil Varma	A 2 4 6 8 A 10 12 14 16 A 18 20 22 24 26 28 30 32 34 36 38
39	219Y1A04E3	S Rahiman	2 4 A 6 8 10 12 14 A 16 18 20 22 24 A 26 28 A A A A 30
40	219Y1A04F3	S Srinath	2 4 6 A 8 10 12 14 16 A 18 20 A 22 24 26 28 30 32 34 36 38
41	219Y1A04F4	S Manasa	A 2 4 6 8 A 10 12 A 14 16 18 20 22 A 24 26 28 30 32 34 36
42	219Y1A04F7	S Srikanth	2 4 6 A 8 10 12 14 16 A 18 20 22 A 24 26 28 30 A 32 34 36
43	219Y1A04F9	T Bhargavi	A A A 2 A 4 6 A 8 10 12 A 14 16 18 A 20 22 24 A 26 28
44	219Y1A04G3	V Prasad Reddy	2 4 A 6 8 10 A 12 14 16 18 20 A A 22 24 26 28 30 32 34 36
45	219Y1A04G6	V Guru Sai Yadav	A A A A A A A

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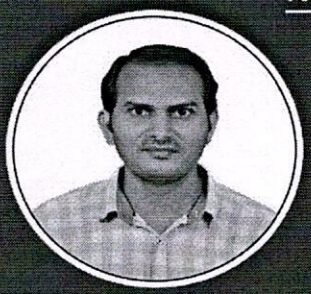
KSNR
lives on..

VALUE ADDED COURSE ON
DESIGN OF VLSI SUBSYSTEMS

RESOURCE PERSONS



Dr. M. MADHUSUDHAN REDDY
ASSOCIATE PROFESSOR IN ECE
KSRM COLLEGE OF ENGINEERING

Smt. K. DIVYA LAKSHMI
ASSISTANT PROFESSOR IN ECE
KSRM COLLEGE OF ENGINEERING

01-05-2024
to
22-06-2024

ORGANIZED BY
DEPARTMENT OF ECE
KSRMCE

ksrmceofficial | www.ksrmce.ac.in | 8143731980, 8575697569

Report of
Value Added Course on "DESIGN OF VLSI SUBSYSTEMS"
From 01/05/2024 to 22/06/2024

Target Group	:	**B.Tech VI-SEM Students**
Details of Participants	:	**51 Students**
Co-coordinator(s)	:	**Sri. P. Subbarayudu**
Resource Person(s)	:	**Dr. M Madhusudhan Reddy, Smt. K. Divya Lakshmi**
Organizing Department	:	**Electronics and Communication Engineering**
Venue	:	**Seminar Hall, SJ Block**

Description:

The Department of Electronics and Communication Engineering conducted a Value Added Course on "Design Of VLSI Subsystems" from 01/05/2024 to 22/06/2024. The course Resource Persons are Dr. M Madhusudhan Reddy and Smt. K. Divya Lakshmi Department of ECE, KSRMCE.

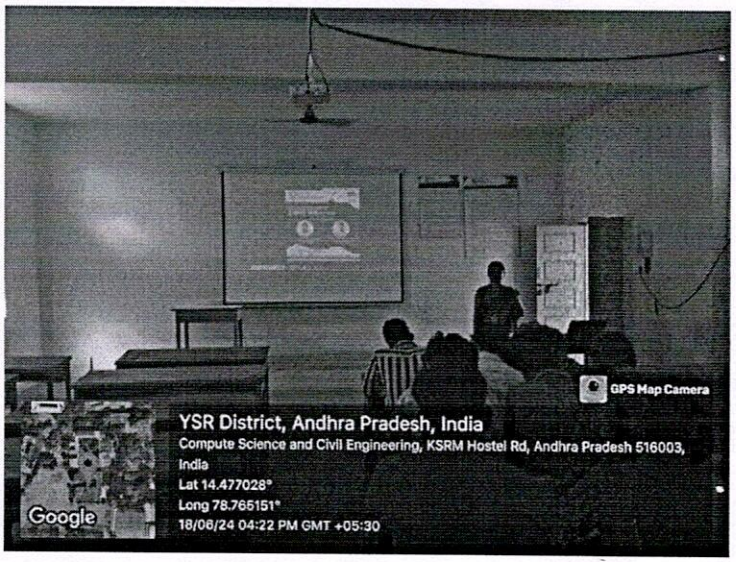
The main objective of this course is to introduce the fundamental concepts of Digital CMOS VLSI subsystem design using design metrics of delay, power, and area in detail. The course focuses more on power estimation, and interconnect aware designs and discusses on few power benefits designs. Approximate computing datapath subsystem designs will be analyzed along with the design, and error metrics. Different forms of standard cell design of latch, and flipflops will be discussed and the importance of timing parameters in sequential circuits will explained.

Design and Analysis of VLSI Subsystems Training include the creation of real-time embedded systems where the end system requirements govern how both the hardware and software components are handled and embedded

With this Certificate course students enhanced their knowledge in the area of VLSI subsystem design and analysis.

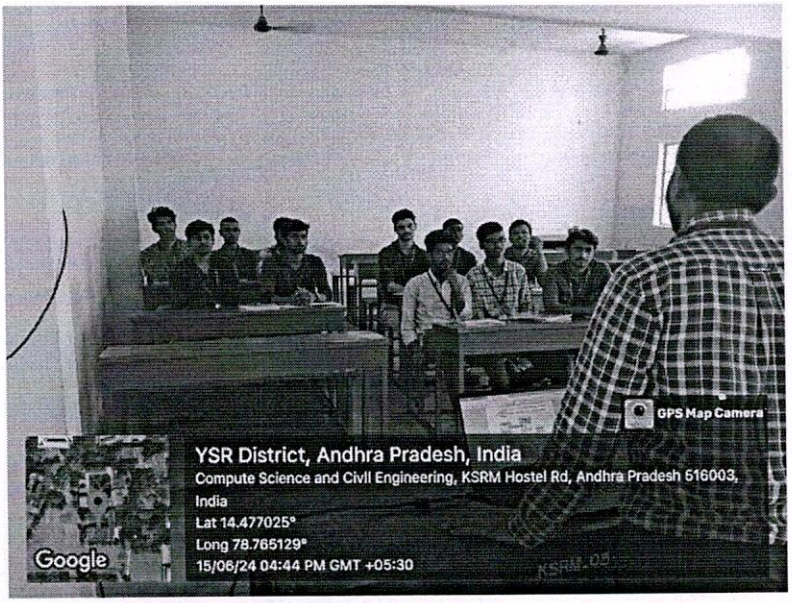
Photos

The pictures taken during the course are given below:



Resource Person Smt. K. Divya Lakshmi, Assist.Prof in ECED,giving lecture on operation of MOSFET

Resource Person Dr. M Madhusudhan Reddy, Assoc.Prof in ECED,giving lecture on design flow of VLSI



Participants Keenly Listening the Lecture

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF MECHANICAL ENGINEERING
VALUE ADDED /CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS"FROM 01/05/2024 to 22/06/2024

ASSESSMENT TEST

Roll Number: _____ **Name of the Student:** _____

Time: 20 Min **(Objective Questions)** **Max.Marks: 20**

Note: Answer the following Questions and each question carries **one** mark.

1. VLSI technology uses _____ to form integrated circuit. { }
a) transistors b) switches c) diodes d) buffers
2. The difficulty in achieving high doping concentration leads to ____{ }_____
a) error in concentration b) error in variation c) error in doping d) distribution error
3. Speed power product is measured as the product of ___{ }_____
a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption
c) gate switching delay and net gate power d) gate power dissipation and absorption
4. nMOS devices are formed in __{ }_____
a) p-type substrate of high doping level b) n-type substrate of low doping level
c) p-type substrate of moderate doping level d) n-type substrate of high doping level
5. In MOS transistors _____ is used for their gate. { }
a) metal b) silicon-di-oxide c) polysilicon d) gallium
6. CMOS inverter has _____ regions of operation.{ }
a) three b) four c) two d) five
7. If p-transistor is conducting and has small voltage between source and drain, then it is said to work in _{ }_____
a) linear region b) saturation region c) non saturation resistive region d) cut-off region
8. Latch-up can be induced by __{ }_____
a) incident radiation b) reflected radiation c) etching d) diffracted radiation
9. Stick diagrams are those which convey layer information through? { }
a) thickness b) color c) shapes d) layers
10. Which color is used for n-diffusion? { }
a) red b) blue c) green d) yellow
11. Which color is used for implant? { }
a) red b) blue c) green d) yellow
12. Circuit design concepts can also be represented using a symbolic diagram. { }
a) true b) false
13. Area A of a slab can be given as ___{ }_____
a) t * W b) t / W c) L * W d) L * t
14. Switch logic is based on { }
a) pass transistors b) transmission gates c) pass transistors and transmission gates d) design rules
15. The switch logic approach takes _____ static current. { }
a) low b) more c) no d) very less
16. The subsystem of the circuits should have _____ interdependence. { }
a) minimum b) maximum c) no d) more

17. Gate logic is also called as { }
a) transistor logic b) switch logic c) complementary logic d) restoring logic
18. Both NAND and NOR gates can be used in gate logic. { }
a) true b) false
19. The CMOS inverter has _____ power dissipation. { }
a) low b) more c) no d) very less
20. Ids depends on _____ { }
a) Vg b) Vds c) Vdd d) Vss

16/20

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF MECHANICAL ENGINEERING
VALUE ADDED /CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS"FROM 01/05/2024 to 22/06/2024

ASSESSMENT TEST

Roll Number: 21K91A0407 **Name of the Student:** A. Bhanu prakash

Time: 20 Min **(Objective Questions)** **Max.Marks: 20**

Note: Answer the following Questions and each question carries **one** mark.

1. VLSI technology uses _____ to form integrated circuit. { a }
a) transistors b) switches c) diodes d) buffers
2. The difficulty in achieving high doping concentration leads to ____{ c }_____
a) error in concentration b) error in variation c) error in doping d) distribution error
3. Speed power product is measured as the product of ___{ a }_____
a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption
c) gate switching delay and net gate power d) gate power dissipation and absorption
4. nMOS devices are formed in __{ a }_____
a) p-type substrate of high doping level b) n-type substrate of low doping level
c) p-type substrate of moderate doping level d) n-type substrate of high doping level
5. In MOS transistors _____ is used for their gate. { c }
a) metal b) silicon-di-oxide c) polysilicon d) gallium
6. CMOS inverter has _____ regions of operation. { c }
a) three b) four c) two d) five
7. If p-transistor is conducting and has small voltage between source and drain, then it is said to work in _{ b }_____
a) linear region b) saturation region c) non saturation resistive region d) cut-off region
8. Latch-up can be induced by __{ c }_____
a) incident radiation b) reflected radiation c) etching d) diffracted radiation
9. Stick diagrams are those which convey layer information through? { b }
a) thickness b) color c) shapes d) layers
10. Which color is used for n-diffusion? { c }
a) red b) blue c) green d) yellow
11. Which color is used for implant? { d }
a) red b) blue c) green d) yellow
12. Circuit design concepts can also be represented using a symbolic diagram. { a }
a) true b) false
13. Area A of a slab can be given as ___{ c }_____
a) t * W b) t / W c) L * W d) L * t
14. Switch logic is based on { d }
a) pass transistors b) transmission gates c) pass transistors and transmission gates d) design rules
15. The switch logic approach takes __a__ static current. { }
a) low b) more c) no d) very less
16. The subsystem of the circuits should have __b__ interdependence. { }
a) minimum b) maximum c) no d) more

17. Gate logic is also called as {d}
a) transistor logic b) switch logic c) complementary logic d) restoring logic
18. Both NAND and NOR gates can be used in gate logic. {c}
a) true b) false
19. The CMOS inverter has _____ power dissipation. {b}
a) low b) more c) no d) very less
20. Ids depends on _____ {d}
a) Vg b) Vds c) Vdd d) Vss

12/20

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF MECHANICAL ENGINEERING
VALUE ADDED /CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS"FROM 01/05/2024 to 22/06/2024

ASSESSMENT TEST

Roll Number: 21941a0432 **Name of the Student:** C. Ajay Kumar

Time: 20 Min **(Objective Questions)** **Max.Marks: 20**

Note: Answer the following Questions and each question carries **one** mark.

1. VLSI technology uses _____ to form integrated circuit. {a}
a) transistors b) switches c) diodes d) buffers
2. The difficulty in achieving high doping concentration leads to ____{c}_____
a) error in concentration b) error in variation c) error in doping d) distribution error
3. Speed power product is measured as the product of ___{a}_____
a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption
c) gate switching delay and net gate power d) gate power dissipation and absorption
4. nMOS devices are formed in __{a }_____
a) p-type substrate of high doping level b) n-type substrate of low doping level
c) p-type substrate of moderate doping level d) n-type substrate of high doping level
5. In MOS transistors _____ is used for their gate. {c}
a) metal b) silicon-di-oxide c) polysilicon d) gallium
6. CMOS inverter has _____ regions of operation.{c}
a) three b) four c) two d) five
7. If p-transistor is conducting and has small voltage between source and drain, then it is said to work in _{ b}_____
a) linear region b) saturation region c) non saturation resistive region d) cut-off region
8. Latch-up can be induced by __{ c}_____
a) incident radiation b) reflected radiation c) etching d) diffracted radiation
9. Stick diagrams are those which convey layer information through? { b }
a) thickness b) color c) shapes d) layers
10. Which color is used for n-diffusion? { c }
a) red b) blue c) green d) yellow
11. Which color is used for implant? { }
a) red b) blue c) green d) yellow
12. Circuit design concepts can also be represented using a symbolic diagram. {a}
a) true b) false
13. Area A of a slab can be given as ___{c }_____
a) t * W b) t / W c) L * W d) L * t
14. Switch logic is based on {c}
a) pass transistors b) transmission gates c) pass transistors and transmission gates d) design rules
15. The switch logic approach takes _____ static current. {a}
a) low b) more c) no d) very less
16. The subsystem of the circuits should have _____ interdependence. {c}
a) minimum b) maximum c) no d) more

17. Gate logic is also called as {c}
a) transistor logic b) switch logic c) complementary logic d) restoring logic
18. Both NAND and NOR gates can be used in gate logic. {a}
a) true b) false
19. The CMOS inverter has _____ power dissipation. {d}
a) low b) more c) no d) very less
20. Ids depends on _____ {c}
a) Vg b) Vds c) Vdd d) Vss

16/20

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF MECHANICAL ENGINEERING
VALUE ADDED /CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS"FROM 01/05/2024 to 22/06/2024

ASSESSMENT TEST

Roll Number: 21 91 1A0415 **Name of the Student:** B. Chinni Krishna.

Time: 20 Min **(Objective Questions)** **Max.Marks: 20**

Note: Answer the following Questions and each question carries **one** mark.

1. VLSI technology uses _____ to form integrated circuit. {a}
a) transistors b) switches c) diodes d) buffers
2. The difficulty in achieving high doping concentration leads to ____{c}_____
a) error in concentration b) error in variation c) error in doping d) distribution error
3. Speed power product is measured as the product of ___{a}_____
a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption
c) gate switching delay and net gate power d) gate power dissipation and absorption
4. nMOS devices are formed in __{a}_____
a) p-type substrate of high doping level b) n-type substrate of low doping level
c) p-type substrate of moderate doping level d) n-type substrate of high doping level
5. In MOS transistors _____ is used for their gate. {c}
a) metal b) silicon-di-oxide c) polysilicon d) gallium
6. CMOS inverter has _____ regions of operation. {c}
a) three b) four c) two d) five
7. If p-transistor is conducting and has small voltage between source and drain, then it is said to work in _{b}_____
a) linear region b) saturation region c) non saturation resistive region d) cut-off region
8. Latch-up can be induced by __{c}_____
a) incident radiation b) reflected radiation c) etching d) diffracted radiation
9. Stick diagrams are those which convey layer information through? { b }
a) thickness b) color c) shapes d) layers
10. Which color is used for n-diffusion? { c }
a) red b) blue c) green d) yellow
11. Which color is used for implant? {d}
a) red b) blue c) green d) yellow
12. Circuit design concepts can also be represented using a symbolic diagram. {a}
a) true b) false
13. Area A of a slab can be given as ___{c}_____
a) t * W b) t / W c) L * W d) L * t
14. Switch logic is based on {d}
a) pass transistors b) transmission gates c) pass transistors and transmission gates d) design rules
15. The switch logic approach takes _____ static current. {a}
a) low b) more c) no d) very less
16. The subsystem of the circuits should have _____ interdependence. {c}
a) minimum b) maximum c) no d) more

17. Gate logic is also called as {a}
a) transistor logic b) switch logic c) complementary logic d) restoring logic
18. Both NAND and NOR gates can be used in gate logic. {a}
a) true b) false
19. The CMOS inverter has _____ power dissipation. { b }
a) low b) more c) no d) very less
20. Ids depends on _____ { c }
a) Vg b) Vds c) Vdd d) Vss

18/20

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF MECHANICAL ENGINEERING
VALUE ADDED /CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS"FROM 01/05/2024 to 22/06/2024

ASSESSMENT TEST

Roll Number: 21 9Y 1A0443 **Name of the Student:** B. Karthik Reddy

Time: 20 Min **(Objective Questions)** **Max.Marks: 20**

Note: Answer the following Questions and each question carries **one** mark.

1. VLSI technology uses _____ to form integrated circuit. {a}
a) transistors b) switches c) diodes d) buffers
2. The difficulty in achieving high doping concentration leads to ____{c}_____
a) error in concentration b) error in variation c) error in doping d) distribution error
3. Speed power product is measured as the product of ___{a}_____
a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption
c) gate switching delay and net gate power d) gate power dissipation and absorption
4. nMOS devices are formed in __{a}_____
a) p-type substrate of high doping level b) n-type substrate of low doping level
c) p-type substrate of moderate doping level d) n-type substrate of high doping level
5. In MOS transistors _____ is used for their gate. {c}
a) metal b) silicon-di-oxide c) polysilicon d) gallium
6. CMOS inverter has _____ regions of operation.{c}
a) three b) four c) two d) five
7. If p-transistor is conducting and has small voltage between source and drain, then it is said to work in _{b}_____
a) linear region b) saturation region c) non saturation resistive region d) cut-off region
8. Latch-up can be induced by __{ c}_____
a) incident radiation b) reflected radiation c) etching d) diffracted radiation
9. Stick diagrams are those which convey layer information through? { b }
a) thickness b) color c) shapes d) layers
10. Which color is used for n-diffusion? {c }
a) red b) blue c) green d) yellow
11. Which color is used for implant? {d}
a) red b) blue c) green d) yellow
12. Circuit design concepts can also be represented using a symbolic diagram. {a}
a) true b) false
13. Area A of a slab can be given as ___{ c }_____
a) t * W b) t / W c) L * W d) L * t
14. Switch logic is based on {a}
a) pass transistors b) transmission gates c) pass transistors and transmission gates d) design rules
15. The switch logic approach takes _____ static current. {a}
a) low b) more c) no d) very less
16. The subsystem of the circuits should have _____ interdependence. { c}
a) minimum b) maximum c) no d) more

17. Gate logic is also called as {d}
a) transistor logic b) switch logic c) complementary logic d) restoring logic
18. Both NAND and NOR gates can be used in gate logic. {a}
a) true b) false
19. The CMOS inverter has _____ power dissipation. { b }
a) low b) more c) no d) very less
20. Ids depends on _____ {d}
a) Vg b) Vds c) Vdd d) Vss

17/20

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF MECHANICAL ENGINEERING
VALUE ADDED /CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS"FROM 01/05/2024 to 22/06/2024

ASSESSMENT TEST

Roll Number: 219Y1A0408 **Name of the Student:** 13. POORNIMA

Time: 20 Min **(Objective Questions)** **Max.Marks: 20**

Note: Answer the following Questions and each question carries **one** mark.

1. VLSI technology uses _____ to form integrated circuit. {a}
a) transistors b) switches c) diodes d) buffers
2. The difficulty in achieving high doping concentration leads to ____{ c}_____
a) error in concentration b) error in variation c) error in doping d) distribution error
3. Speed power product is measured as the product of ___{a}_____
a) gate switching delay and gate power dissipation b) gate switching delay and gate power absorption
c) gate switching delay and net gate power d) gate power dissipation and absorption
4. nMOS devices are formed in __{ a }_____
a) p-type substrate of high doping level b) n-type substrate of low doping level
c) p-type substrate of moderate doping level d) n-type substrate of high doping level
5. In MOS transistors _____ is used for their gate. { c}
a) metal b) silicon-di-oxide c) polysilicon d) gallium
6. CMOS inverter has _____ regions of operation.{c }
a) three b) four c) two d) five
7. If p-transistor is conducting and has small voltage between source and drain, then it is said to work in _{b}_____
a) linear region b) saturation region c) non saturation resistive region d) cut-off region
8. Latch-up can be induced by __{c}_____
a) incident radiation b) reflected radiation c) etching d) diffracted radiation
9. Stick diagrams are those which convey layer information through? { b }
a) thickness b) color c) shapes d) layers
10. Which color is used for n-diffusion? { c}
a) red b) blue c) green d) yellow
11. Which color is used for implant? {d}
a) red b) blue c) green d) yellow
12. Circuit design concepts can also be represented using a symbolic diagram. {a}
a) true b) false
13. Area A of a slab can be given as ___{ c}_____
a) t * W b) t / W c) L * W d) L * t
14. Switch logic is based on {d}
a) pass transistors b) transmission gates c) pass transistors and transmission gates d) design rules
15. The switch logic approach takes _____ static current. {a}
a) low b) more c) no d) very less
16. The subsystem of the circuits should have _____ interdependence. {b}
a) minimum b) maximum c) no d) more

17. Gate logic is also called as {a}
a) transistor logic b) switch logic c) complementary logic d) restoring logic
18. Both NAND and NOR gates can be used in gate logic. {b}
a) true b) false
19. The CMOS inverter has _____ power dissipation. {b}
a) low b) more c) no d) very less
20. Ids depends on _____ {C}
a) Vg b) Vds c) Vdd d) Vss

K.S.R.M. COLLEGE OF ENGINEERING (AUTONOMOUS), KADAPA-516003
DEPARTMENT OF ECE
VALUE ADDED/CERTIFICATE COURSE ON
"DESIGN OF VLSI SUBSYSTEMS" FROM 01/05/2024 to 22/06/2024

AWARD LIST

S.NO	Roll Number	Name of the Student	Marks Obtained
1	219Y1A0407	A Bhanu Prakash	16
2	219Y1A0408	B Poornima	17
3	219Y1A0413	B Karthik Reddy	18
4	219Y1A0418	B Chinni Krishna	16
5	219Y1A0421	C Vasanth Kumar Reddy	17
6	219Y1A0423	C Pavan Kalyan	18
7	219Y1A0426	C Kiran Kumar	16
8	219Y1A0427	C Renuka	14
9	219Y1A0428	C Ravikumar	18
10	219Y1A0429	C Kishore Kumar	17
11	219Y1A0432	C Ajay Kumar	12
12	219Y1A0433	C Usuvandla Akhil	18
13	219Y1A0435	D Srija	15
14	219Y1A0443	D Naga Lakshmi	15
15	219Y1A0444	G Sai Konda Reddy	18
16	219Y1A0446	G Prem Kumar	16
17	219Y1A0449	G Ganesh	17
18	219Y1A0450	G Venkata Krishna	15
19	219Y1A0461	K Hari Krishna Reddy	15
20	219Y1A0465	K Sai Narasimha	15
21	219Y1A0469	K Radha Priyanjali	15
22	219Y1A0479	Kunduru Praveen	18

23	219Y1A0481	K Sindhu Priya	17
24	219Y1A0483	K Mallesh	16
25	219Y1A0496	M Obulamma	15
26	219Y1A0495	M. Mallikarjuna	15
27	219Y1A0499	M Diwakar Reddy	18
28	219Y1A04A0	M Sai Ram Naik	18
29	219Y1A04A8	N Gari Hanumanth Reddy	12
30	219Y1A04B0	N Divakar	13
31	219Y1A04B6	N Vishnuvardhan Reddy	14
32	219Y1A04C0	O Naveen Kumar	12
33	219Y1A04C2	P Vijaya Shimha Prasad	13
34	219Y1A04C5	P Satya Narayana Reddy	15
35	219Y1A04C6	P Chandana (W)	18
36	219Y1A04C7	P Manideep Reddy	17
37	219Y1A04D0	P Devendra	16
38	219Y1A04E1	S Venkata Nikhil Varma	15
39	219Y1A04E3	S Rahiman	15
40	219Y1A04F3	S Srinath	18
41	219Y1A04F4	S Manasa	18
42	219Y1A04F7	S Srikanth	12
43	219Y1A04F9	T Bhargavi	13
44	219Y1A04G3	V Prasad Reddy	17
45	219Y1A04G6	V Guru Sai Yadav	16
46	229Y5A0407	G Anjitha	17
47	229Y5A0418	T Sindhu	16
48	229Y5A0419	T Manikanta	15

49	229Y5A0420	T Anil Kumar	15
50	229Y5A0422	V Bhanu Venkata Prakash	18
51	229Y5A0423	S Ganga Harish	18

Coordinator

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

K.S.R.M. COLLEGE OF ENGINEERING

(UGC - Autonomous)
Kadapa, Andhra Pradesh, India– 516 003
Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

KSNR
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Certificate of Completion

This to certify that Mr/Mrs._____Bearing the Roll Number_____has Successfully Completed Value AddedCourse on "Design of VLSI subsystems" from 1st, May 2024 to 22nd june 2024, Organized by Department of Electronics and Communication Engineering, KSRMCE, Kadapa.

Coordinator HOD ECE Principal

K.S.R.M. COLLEGE OF ENGINEERING

(UGC - Autonomous)
Kadapa, Andhra Pradesh, India– 516 003
Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

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Certificate of Completion

This to certify that ~~Mr~~/Mrs. B. Poornima Bearing the Roll Number 219Y1A0408 has Successfully Completed Value AddedCourse on "Design of VLSI subsystems" from 1st, May 2024 to 22nd june 2024, Organized by Department of Electronics and Communication Engineering, KSRMCE, Kadapa.

Coordinator

HOD ECE

Principal

K.S.R.M. COLLEGE OF ENGINEERING

(UGC - Autonomous)
Kadapa, Andhra Pradesh, India– 516 003
Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

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Certificate of Completion

This to certify that Mr/~~Mrs~~. B. Karthik Reddy Bearing the Roll Number 219Y1A0413 has Successfully Completed Value Added Course on "Design of VLSI subsystems" from 1st, May 2024 to 22nd June 2024, Organized by Department of Electronics and Communication Engineering, KSRMCE, Kadapa.

Coordinator HOD ECE Principal

K.S.R.M. COLLEGE OF ENGINEERING

(UGC - Autonomous)
Kadapa, Andhra Pradesh, India– 516 003
Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

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Certificate of Completion

This to certify that Mr/~~Mrs~~. A. Bhanu Prakash Bearing the Roll Number 219Y1A0407 has Successfully Completed Value Added Course on "Design of VLSI subsystems" from 1st, May 2024 to 22nd june 2024, Organized by Department of Electronics and Communication Engineering, KSRMCE, Kadapa.

Coordinator HOD ECE Principal

Feedback form on Value Added Course "Design of VLSI Subsystems" from **01/05/2024 to 22/06/2024**

* Indicates required question

1. Name of the student *

_____

2. Roll No. *

_____

3. The objectives of the Value Added Course were met (Objective) *

Mark only one oval.

- ◯ Excellent
- ◯ Good
- ◯ Satisfactory
- ◯ Poor

4. The content of the course was organized and easy to follow (Delivery) *

Mark only one oval.

- ◯ Excellent
- ◯ Good
- ◯ Satisfactory
- ◯ Poor

5. The Resource Persons were well prepared and able to answer any question (Interaction) *

Mark only one oval.

- ◯ Excellent
- ◯ Good
- ◯ Satisfactory
- ◯ Poor

6. The exercises/role play were helpful and relevant (Syllabus Coverage) *

Mark only one oval.

- ◯ Excellent
- ◯ Good
- ◯ Satisfactory
- ◯ Poor

7. The Value Added Course satisfy my expectation as a value added Programme (Course Satisfaction) *

Mark only one oval.

- ◯ Excellent
- ◯ Satisfactory
- ◯ Good
- ◯ Poor

8. Any issues

_____

Name of the student	Roll No.	The objectives of the Value Added Course were met (Objective)	The content of the course was organized and easy to follow (Delivery)	The Resource Persons were well prepared and able to answer any question (Interaction)	The exercises/role play were helpful and relevant (Syllabus Coverage)	The Value Added Course satisfy my expectation as a value added Programme (Course Satisfaction)	Any issues
G. Venkata krishna	219y1a0450	Excellent	Excellent	Excellent	Excellent	Excellent	
P.manideep reddy	219Y1A04C7	Excellent	Excellent	Excellent	Excellent	Excellent	No issues
N divakar	219y1a04b0	Good	Excellent	Good	Good	Satisfactory	
Srinath	219y1a04f3	Good	Good	Good	Good	Good	
D.Naga lakshmi	219y1a0443	Good	Good	Good	Satisfactory	Good	No
Sayyad Rahiman	219y1a04e3	Satisfactory	Satisfactory	Satisfactory	Satisfactory	Good	
K.Radha priyanjali	219y1A0469	Good	Satisfactory	Good	Satisfactory	Satisfactory	No
K.praveen	219y1A0479	Satisfactory	Good	Good	Good	Satisfactory	No
P. Chanadana	219y1a04c6	Good	Good	Good	Good	Good	No issues
B.Vishnuvardhan Reddy	219y1a0410	Good	Satisfactory	Satisfactory	Satisfactory	Satisfactory	No
Diwakar Reddy	219y1a0499	Excellent	Excellent	Excellent	Excellent	Excellent	.
V. Bhanu venkata prakash	229Y5A0422	Excellent	Excellent	Excellent	Excellent	Excellent	No
C.Renuka	219y1a0427	Satisfactory	Good	Good	Good	Good	
Reddy Prasad	219y1a04g3	Good	Good	Excellent	Excellent	Satisfactory	No
T.Manikanta	229Y5A0419	Satisfactory	Good	Satisfactory	Satisfactory	Good	No
D.snehitha	219y1a0439	Satisfactory	Satisfactory	Satisfactory	Satisfactory	Satisfactory	No
Dasari Prasanna	219y1a0438	Good	Good	Good	Good	Good	Ntg
T bhargavi	219y1a04f9	Good	Good	Good	Good	Satisfactory	No issues

B Poornima	219y1a0408	Excellent	Excellent	Excellent	Excellent	Excellent	
M. obulamma	219y1a0496	Good	Good	Good	Good	Good	No
Golla Anjitha	229y5a0407	Good	Good	Good	Good	Good	
S Srikanth	219y1a04f7	Excellent	Excellent	Excellent	Excellent	Excellent	No issues
K. Anithakumari	219y1a0459	Excellent	Excellent	Excellent	Good	Excellent	
N. HanumanthReddy	219y1a04a8	Excellent	Good	Good	Good	Good	No
P DEVENDRA	219y1a04d0	Good	Good	Excellent	Good	Excellent	NO
O.Naveen Kumar	219y1a04c0	Good	Good	Excellent	Excellent	Satisfactory	No issues
Manupati mallikarjuna	219Y1A0495	Good	Good	Good	Good	Excellent	
Shaik arshad	219Y1A04E4	Good	Good	Good	Good	Good	Nil
K.Sai Narasimha	219y1a0465	Excellent	Good	Good	Good	Satisfactory	No
N.bhanu	219y1a04a5	Good	Good	Excellent	Good	Good	No issues
S.Ganga Harish	229Y5A0423	Excellent	Good	Good	Excellent	Satisfactory	NO
CHINTHALA RAVI KUMAR	219y1a0428	Excellent	Good	Excellent	Excellent	Good	No

UNIT-3 Basic Circuit concepts

Typical sheet resistance R_s of MOS layers

Layer	R_s ohm per square		
	5μm	2μm	1·2μm
Metal	0·03	0·04	0·04
Diffusion	10→50	20→45	20→45
Silicide	2→4	—	—
Polysilicon	15→100	15→30	15→30
n-transistor channel	10^4	2×10^4	2×10^4
P-transistor channel	2.5×10^4	4.5×10^4	4.5×10^4

NOTE:-1) In some processes a silicide layer is used in place of polysilicon.

2) The figures given are for n-diffusion regions. The values for P-diffusion are 2.5 times these values. These values are approximations only.

Sheet Resistance (R_s):-

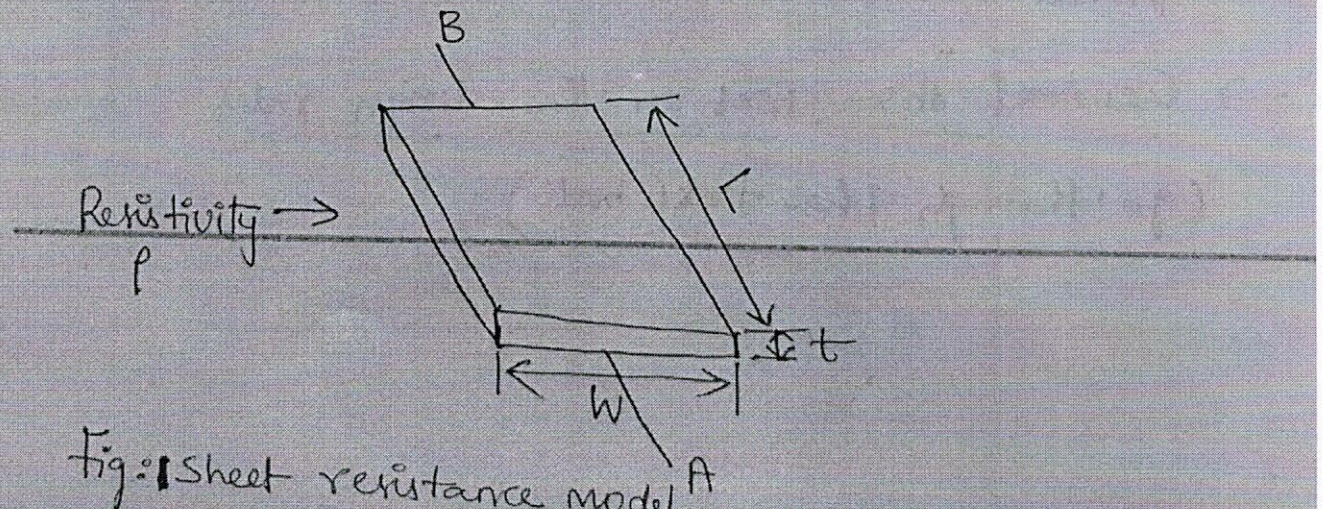


Fig:1 Sheet resistance model

Consider a uniform slab of conducting material of

resistivity ρ, width W, thickness t, and length between faces L. The arrangement is shown in Fig:1

Consider the resistance R_{AB} between two opposite faces.

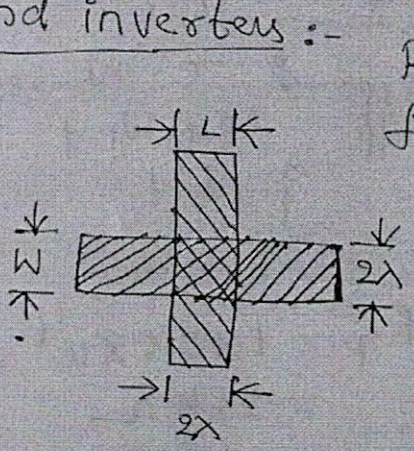
$$R_{AB} = \frac{\rho L}{A} \text{ ohm}$$

where A = cross-section area $= W \times t$ $\left(\because \frac{L}{W}\right)$

Thus $R_{AB} = \frac{\rho L}{tW}$ ohm $= \frac{L}{W} \times \frac{\rho}{t}$ ohm $= Z \times R_S$

where $R_S = \frac{\rho}{t}$ = ohm per square (or sheet resistance)

Sheet Resistance concept applied to MOS transistors and inverters :-



(a) nMOS transistor having

$L = 2\lambda$, $W = 2\lambda$

$\therefore Z = \frac{L}{W} = \frac{2\lambda}{2\lambda} = 1$ Square slab

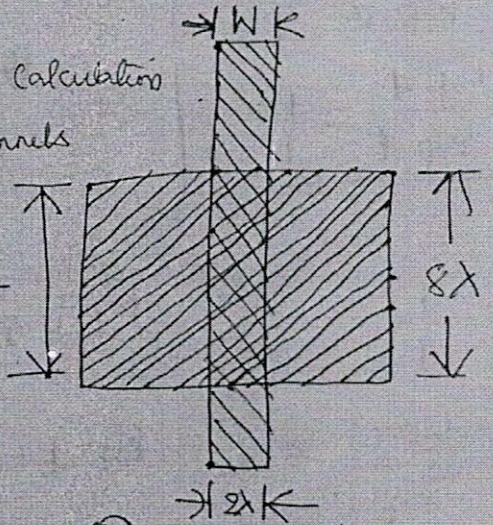
$\therefore$ Resistance $R = Z \times R_{sn}$

→ (for 5μm technology) = 1 Square × R_S $\frac{\text{ohm}}{\text{Square}}$

$= 1 \times 10^4 = \underline{10 k\Omega}$

→ for 2μm technology $= 1 \times 2 \times 10^4 = \underline{20 k\Omega}$

Resistance Calculation for two Channels



(b) nMOS transistor having

$L = 8\lambda$, $W = 2\lambda$

$\therefore Z = \frac{L}{W} = \frac{8\lambda}{2\lambda} = 4$

Resistance $R = Z \times R_{sn}$

(for 5μm) $= 4 \times 10^4$

$= \underline{40 k\Omega}$

(2μm) $R = 4 \times 2 \times 10^4$

$= \underline{80 k\Omega}$

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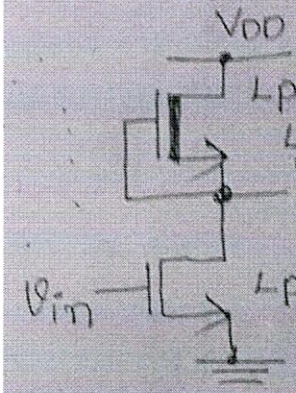
nMOS inverter (4:1) (5µm technology) cmos inverter (1:1)



$R_{p.u} = Z_{pu} \cdot R_{sn} = 4 \times 10^4\ \Omega = 40k\Omega$

$R_{p.d} = Z_{p.d} \cdot R_{sn} = 1 \times 10^4\ \Omega = 10k\Omega$

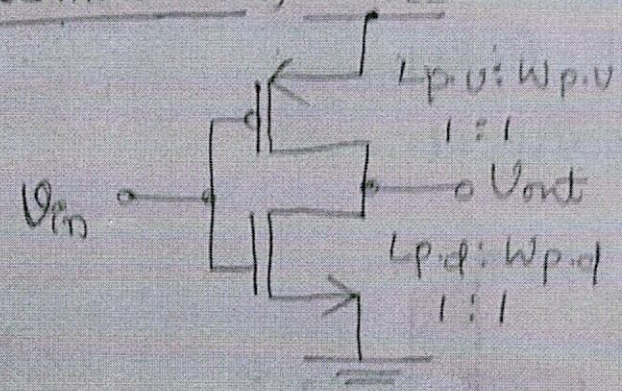
$R = R_{p.u} + R_{p.d} = 40k\Omega + 10k\Omega = 50k\Omega$

$\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$

$Z_{pu} = \frac{L_{p.u}}{W_{p.u}} = \frac{4}{1}$

$Z_{pd} = \frac{L_{p.d}}{W_{p.d}} = \frac{1}{1}$

cmos inverter (1:1)



$\frac{Z_{pu}}{Z_{pd}} = \frac{1}{1}$

$Z_{pu} = \frac{L_{p.u}}{W_{p.u}} = \frac{1}{1}$

$Z_{p.d} = \frac{L_{p.d}}{W_{p.d}} = \frac{1}{1}$

$R_{p.u} = Z_{p.u} \cdot R_{sp} = 1 \times 2.5 \times 10^4\ \Omega = 25k\Omega$

$R_{pd} = Z_{pd} \cdot R_{sn} = 1 \times 10^4\ \Omega = 10k\Omega$

$R = R_{p.u} + R_{p.d} = 25k\Omega + 10k\Omega = 35k\Omega$

Area capacitances of layers :-

for any layer, knowing the dielectric (SiO_2) thickness, we can calculate area capacitances as follows:

$$C = \frac{\varepsilon_0 \varepsilon_{ins} A}{D} \text{ Farads} \quad (A = \text{area} = W \times L)$$

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where D = thickness of SiO_2

A = Area of plates

ε_{ins} = relative permittivity of $SiO_2 \doteq 4.0$

$\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm (permittivity of free space)

Typical values of area capacitance are set out in Table 1 for 5μm technology, 2μm and 1.2μm technologies.

Capacitance	Value in $pF \times 10^{-4}/\mu m^2$ (Relative values in bracket)		
	5 μm	2μm	1.2μm
Gate to channel	4 (1.0)	8 (1.0)	16 (1.0)
Diffusion (active)	1 (0.25)	1.75 (0.22)	3.75 (0.23)
polysilicon to Substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.038)
Metal 1 to substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
Metal 2 to substrate	0.2 (0.05)	0.17 (0.02)	0.17 (0.01)
Metal 2 to metal 1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
Metal 2 to polysilicon	0.3 (0.075)	0.3 (0.038)	0.3 (0.018)

Note: Relative value = specified value / gate to channel value for that technology

Standard unit of capacitance $\square C_g$:-

The unit is denoted $\square C_g$ and is defined the gate-to-channel capacitance of a MOS transistor having W = L = feature size, that is, a standard (or 'feature size' square ($2\lambda \times 2\lambda$ for λ-based rules).

Metal area / standard gate to channel area

$\square C_g$ = Relative area × Relative C value

→ Relative area is defined as the ratio between the area of

Metal capacitance C_m = Relative area × Relative c value

$$= \frac{100\lambda \times 3\lambda}{2\lambda \times 2\lambda} \times 0.075$$

$$= 75 \times 0.075 = 5.625 \square_{cg}$$

Polysilicon capacitance $C_p = \frac{4\lambda \times 4\lambda + 3\lambda \times 2\lambda}{2\lambda \times 2\lambda} \times 0.1 \square_{cg}$

$$= 0.55 \square_{cg}$$

Gate capacitance $C_g = \frac{2\lambda \times 2\lambda}{2\lambda \times 2\lambda} \times 1.0 \square_{cg}$

$$= 1 \square_{cg}$$

Total capacitance $C_T = C_m + C_p + C_g = 5.625 + 0.55 + 1$

$$= 7.175 \square_{cg}$$

Choice of layers :—

*In designing a circuit to meet the given specifications, there are several possible ways in which the requirements may be met, including the choice b/w the layers on which to route certain data and control signals. However, there a certain commonsense constraints which should be considered.

① V_{DD} and V_{SS} (GND) should be connected using metal layers wherever possible.

② long lengths of polysilicon should be used only after careful consideration.

③ Capacitive effects must also be carefully considered.

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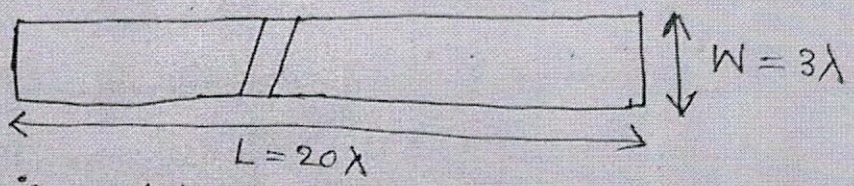
interest and the standard gate area ($2\lambda \times 2\lambda$ for λ-based rules) .

(1)



Consider the area in metal 1 to substrate capacitance (5µm technology)

$$\square C_g = \text{relative area} \times \text{relative } C \text{ value}$$

$$= \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} \times 0.075$$

$$= 15 \times 0.075$$

$$= 1.125$$

(2) Consider the area in polysilicon to substrate capacitance (5µm)

$$\square C_g = \text{Relative area} \times \text{relative } C \text{ value}$$

$$= \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} \times 0.1$$

$$= 15 \times 0.1$$

$$= 1.5 \square C_g$$

Example :-

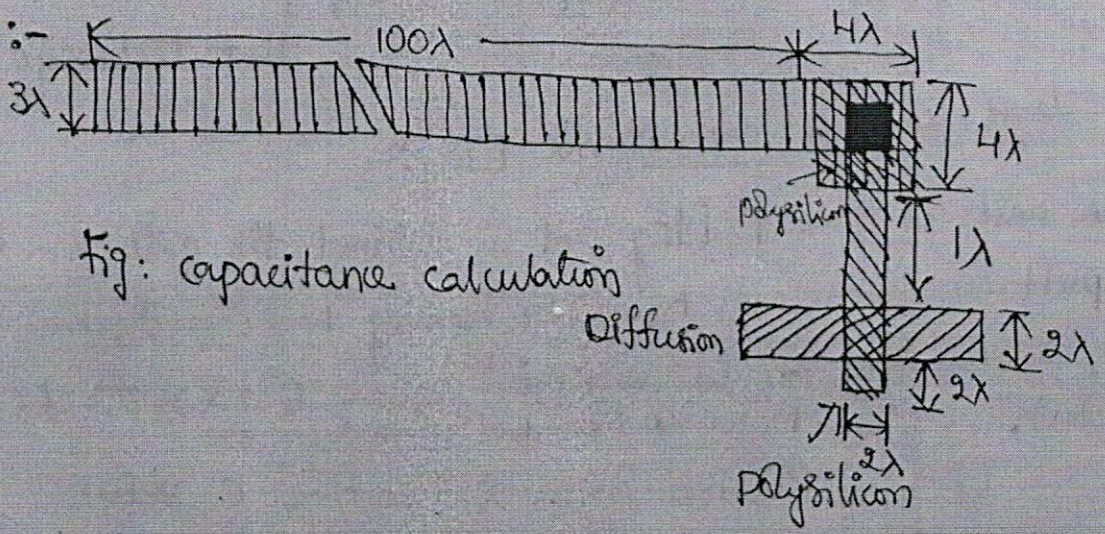


Fig: capacitance calculation

Peripheral capacitance :-

* The source and drain n-diffusion regions form junctions with the p-substrate (or p-well at well-defined and uniform depths. Similarly for p-diffusion regions form junctions with the n-substrate (or n-well at well-defined and uniform depths.
* for diffusion regions, each diode thus formed has associated with it a peripheral (side-wall) capacitance in pF per unit length which can be considerably greater than the area capacitance of the diffusion region to substrate.
* The smaller the source and drain area, the greater becomes the relative value of the peripheral capacitance.

Propagation Delays :-

1) Cascaded pass transistors :-

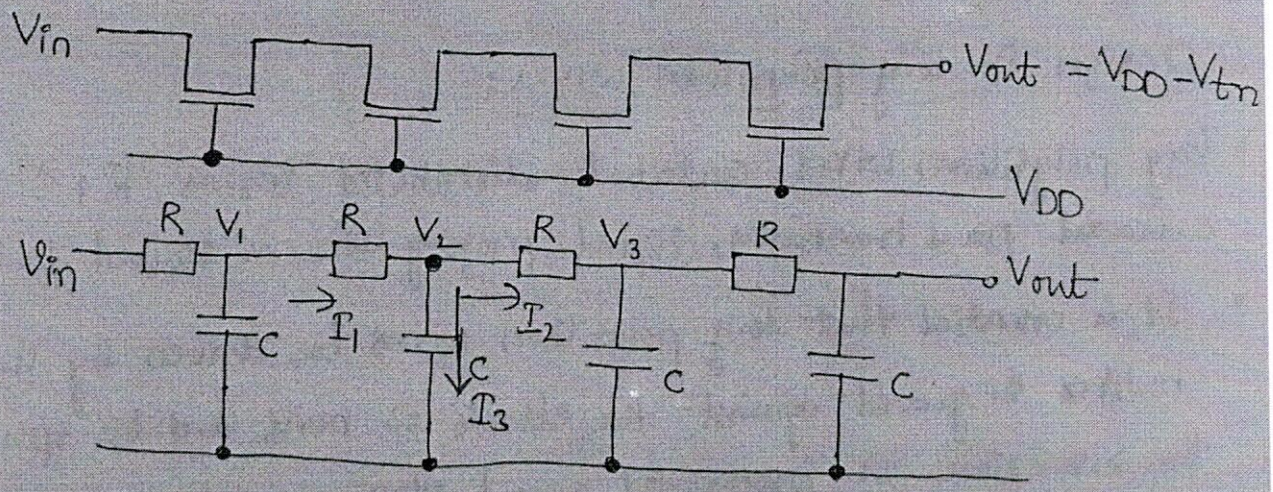


Fig: Propogation delays in pass transistor chain

Where R = resistance per unit length
C = capacitance per unit length
x = distance along network from input.

The propagation time T_p for a signal to propagate a distance x is

$$T_p \propto x^2$$

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③ Charge sharing may also cause problems in certain circuits (or architectures and must be carefully considered.

Choice of layers

Layer	Resistance	Capacitance
metal	low	low
polysilicon	high	moderate
Diffusion (active)	moderate	high

Wiring capacitances

The area capacitances associated with the layers to substrate and from gate to channel. There are other significant sources of capacitance which contribute to the overall wiring capacitance.

① Fringing fields :—

* capacitance due to fringing field effects can be a major compone of the overall capacitance of interconnect wires.
* If accurate prediction of performance is needed, then fringing field capacitance (C_{ff}) should be taken into account.

② Interlayer capacitances :—

* The parallel plate effects are present between one layer and another.
* for a given area, metal to polysilicon capacitance must be higher than metal to substrate.
* The interlayer capacitance is highly dependent on layout.

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$$I_1 = I_2 + I_3 \quad (\text{at node } V_2)$$

$$I_3 = I_1 - I_2$$

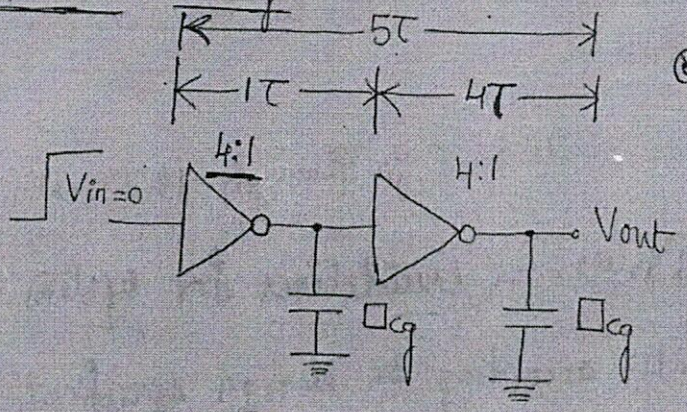
The response at node V_2 w.r.to time is given by

$$C\frac{dV_2}{dt} = \frac{[(V_1 - V_2) - (V_2 - V_3)]}{R}$$

As the no of sections in such a network becomes large, this expression reduces to

$$RC\frac{dV}{dt} = \frac{d^2V}{dx^2}$$

Inverter delays :-



* The inverter pair delay for inverters having 4:1 ratio is 5τ

Fig ① nMOS inverter pair delay.

- If we consider a pair of cascaded inverters, then the delay over the pair will be $\tau + 4\tau = 5\tau$.
- The delay through a pair of similar nMOS inverters is

$$\tau_d = \left(1 + \frac{Z_{p.u}}{Z_{p.d}}\right)\tau$$

- The gate capacitance ($= 2\square C_g$) is double that of the comparable nMOS inverter since the input to a CMOS inverter is connected to both transistor gates.

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The analysis can be simplified if all R & C are lumped together, then $R_{total} = n \cdot \gamma \cdot R_s$

$$C_{total} = n \cdot c \cdot \square c_g$$

where γ = relative resistance per section in terms of R_s and

c = relative capacitance per section in terms of $\square c_g$.

Then, the overall delay τ_d for n sections is given by

$$\tau_d = n^2 \cdot \gamma \cdot c(\tau)$$

* Thus, the overall delay increases rapidly as n increases and in practice no more than four pass transistors should be normally connected in series.
* However, this number can be exceeded if a buffer is inserted b/w each group of 4 pass transistors, otherwise if relatively long time delays are acceptable.

2) Design of long polysilicon wires:-

* long polysilicon wires contribute distributed series R & C for cascaded pass transistors, signal propagation is slowed down.
* It is essential that long polysilicon wires be driven by suitable buffers to guard against the effects of noise and to speed up the rise-time of propagated signal edges.

The delay unit(τ):-

Time constant $\tau = (\Sigma R_s) \times \square C_g$ — standard unit of capacitance $pF \times 10^{-4}/\mu m^2$

$$= \left\{ \left(\frac{L}{W} R_s \right) \times \square C_g \right\} \text{ Seconds}$$

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Sources of power dissipation :-

There are different sources of power dissipation in CMOS logic circuits.

1) Dynamic power consumption :-

In a CMOS logic circuit, power is dissipated during the transition of the output node capacitance.

During the low-high transition, the output capacitor is charged through the pMOS transistor and during the high-low transition, the output capacitor is discharged through the nMOS transistor.

dynamic power dissipation is also called the switching power dissipation, caused by the charging and discharging of the node capacitance as shown in fig.

This is the dominant source of power consumption in CMOS system-on-chip (SoC), accounting for roughly 75% of the total. (80% - 90%)

It is generally represented by the following approximation,

$$P_{dynamic} = \alpha C_L V_{dd}^2 f_{clk} \rightarrow (1)$$

Where α = switching activity factor

C_L = overall capacitance to be charged and discharged in a reference clock cycle.

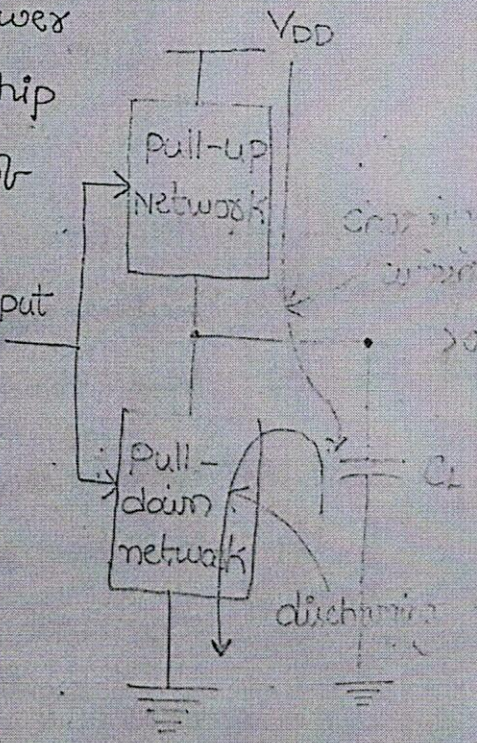

Fig. Switching power dissipation.

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V_{dd} = Supply voltage

f_{clk} = Switching frequency of a global clock

from eq① It is clear that the switching power is entirely dependent on the power supply voltage, the load capacitance and the switching frequency. It is independent of the dimensions of transistors. If we minimize the ~~power~~ supply voltage of the (given) circuit, we can (or) reduce the reduce the switching power consumption.

2) Short-circuit power dissipation :-

During the transition of the input signal due to (the) finite rise (or) fall times, there is always a short-circuit path blw V_{DD} and the ground. So there is a short-circuit power dissipation and it is given by

$$P_{sc} = I_{mean} \cdot V_{DD}$$

$$P_{sc} = t_{sc} V_{DD} I_{peak} f$$

$$P_{s/c} = I_{sc} \cdot V_{DD}$$

Where t_{sc} is the time for which both nMOS and pMOS transistors are ON simultaneously, and I_{peak} is the maximum Saturation current that flows through the transistors.

This type of power dissipation can be controlled by minimizing the transition times on nets. It usually accounts for 15% - 20% of the overall power dissipation.

(10%-15%)

$\left(\frac{W}{L}\right)_{pMOS}$ = $\left(\frac{W}{L}\right)_{nMOS}$

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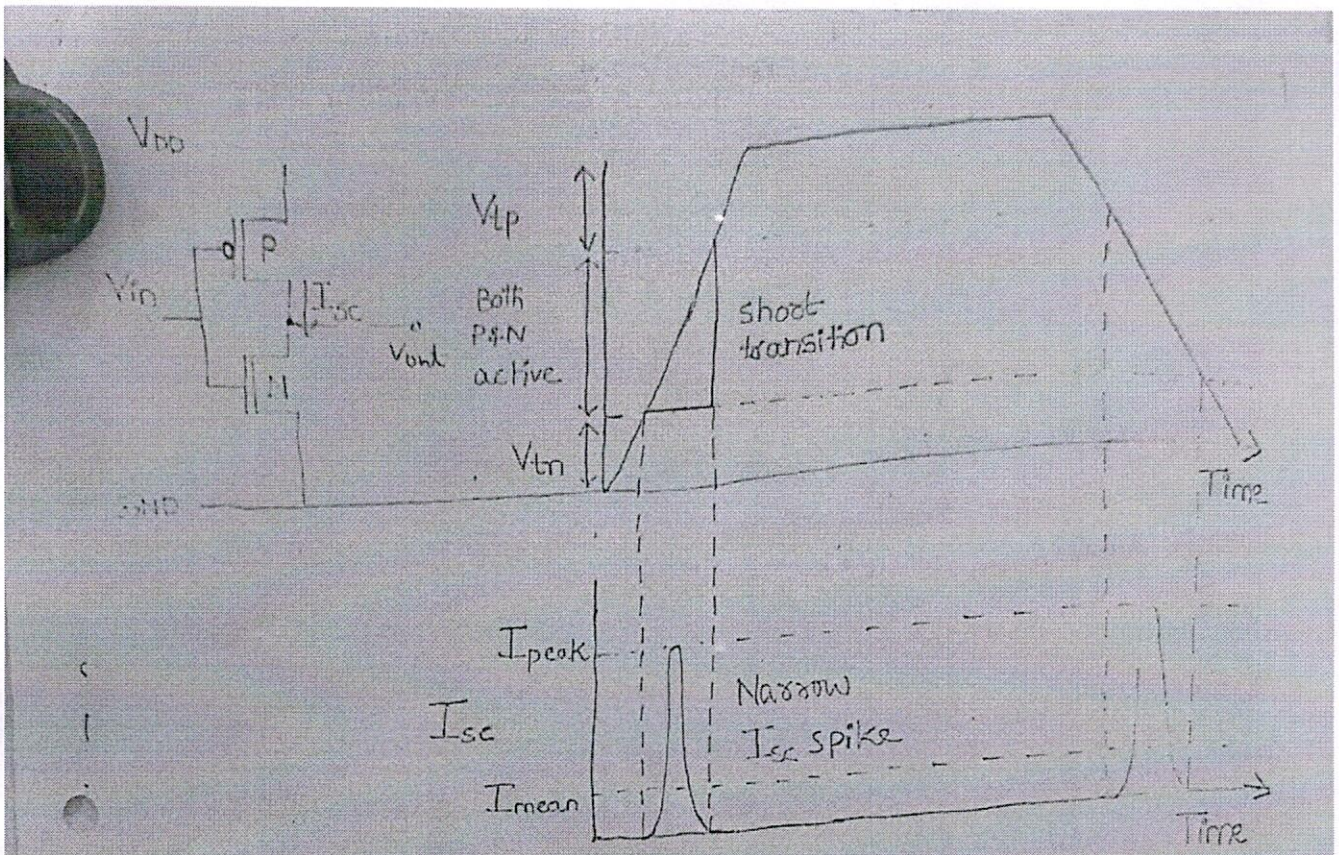

Fig. Short-circuit current.

(3) Static power dissipation:— (due to reverse bias junction leakage)

The Static power dissipation is always present due to the leakage current of the transistors even if the circuit is not switching. This is also known as leakage power dissipation and is given by (10% - 30%)

$$P_{static} = I_{leakage} \cdot V_{DD}$$

where $I_{leakage}$ is the leakage current that flows b/w V_{DD} and the ground.

This component becomes a larger problem as device geometries shrink and transistor threshold voltages (V_t) drop.

Leakage current depends up on the supply (V_{dd}) V_t itself, transistor aspect ratio (W/L) and temp...

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The leakage current of a transistor is mainly the result of reverse-biased PN Junction leakage, Subthreshold leakage and gate leakage is shown in Fig.

Leakage is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology.

To reduce leakage power, many techniques have been proposed, including dual-Vth, multi-Vth, optimal standby input vector Selection, transistor stacking and body bias.

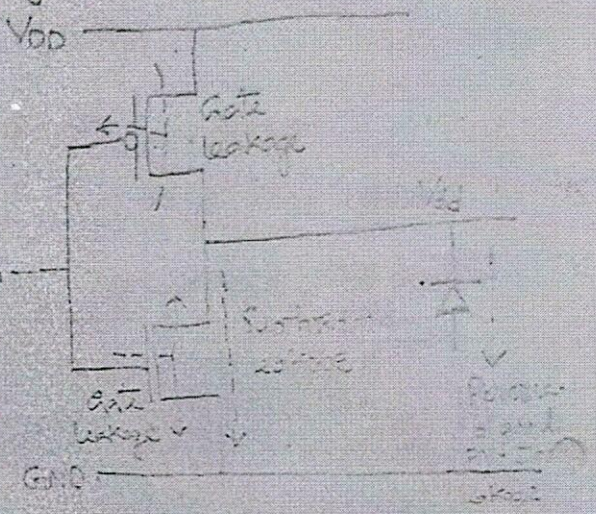

Fig. leakage currents in an inverter

Contribution of different power dimpation :-

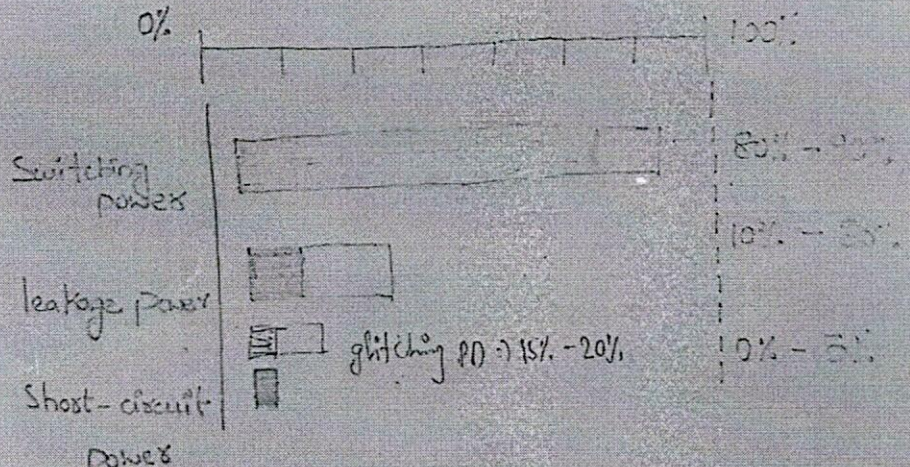

fig. contribution of different powers.

The total power dissipation of a CMOS ckt is the sum of these three power dissipations and can be expressed as.

$$P_{total} = P_{dynamic} + P_{sc} + P_{static}$$

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Note that there is also an additional overhead which consists of the input routing capacitance, all of which are increasing functions of N. If this overhead is neglected, the amount of power reduction achievable in a N-block parallel implementation is

$$\frac{P_{parallel}}{P_{reference}} = \frac{V_{DD,new}^{\ 2}}{V_{DD}^{\ 2}} \cdot \left(1 + \frac{C_{reg}}{C_{total}}\right)$$

The lower bound of switching power reduction realizable with architecture-driven voltage scaling is found, assuming zero threshold voltage, as

$$\frac{P_{parallel}}{P_{reference}} \geq \frac{1}{N^2}$$

Two obvious consequences of this approach are the increased area and the increased latency. A total of N identical processing blocks must be used to slow down the operation (clocking) speed by a factor of N. In fact, the silicon area will grow even faster than the number of processors because of signal routing and the overhead circuitry. The timing diagram in Fig shows that the parallel implementation has a latency of N clock cycles, as in the N-stage pipelined implementation. Considering its smaller area overhead, however, the pipelined approach offers a more efficient alternative for reducing the power dissipation while maintaining the throughput.

Reduction of Switched Capacitance

It was already established in the previous sections that the amount of switched capacitance plays a significant role in the dynamic power dissipation of the circuit. Hence, reduction of this parasitic capacitance is a major goal for low-power design of digital integrated circuits. In this Section, we will consider various techniques at the system level, circuit level and physical design (mask) level which can be used to reduce the amount of switched capacitance.

a] *System-Level Measures*

At the system level, one approach to reduce the switched capacitance is to limit the use of shared resources. A simple example is the use of a global bus structure for data transmission between a large number of operational modules . If a single shared bus is connected to all modules as in fig. this structure results in a large bus capacitance due to (i) the large number of drivers and receivers sharing the same transmission medium, and (ii) the parasitic capacitance of the long bus line. Obviously, driving the large bus capacitance will require a significant amount of power consumption during each bus access. Alternatively, the global bus structure can be partitioned into a number of smaller dedicated local buses to handle the data transmission between neighboring modules, as shown in Fig. In this case, the switched capacitance during each bus access is significantly reduced, although multiple buses may increase the overall routing area on the chip.

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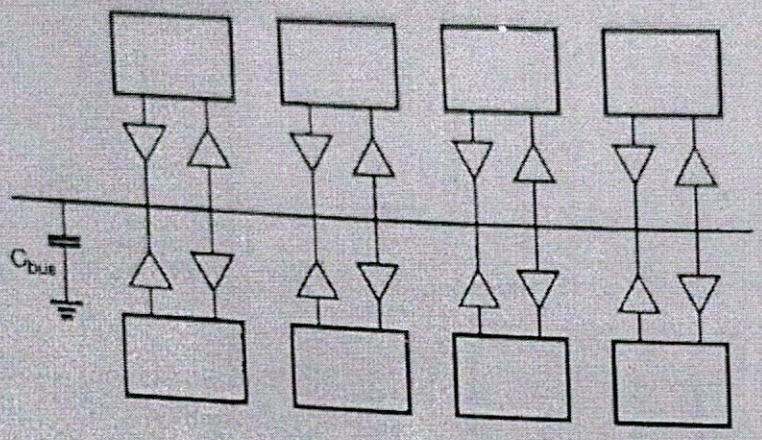
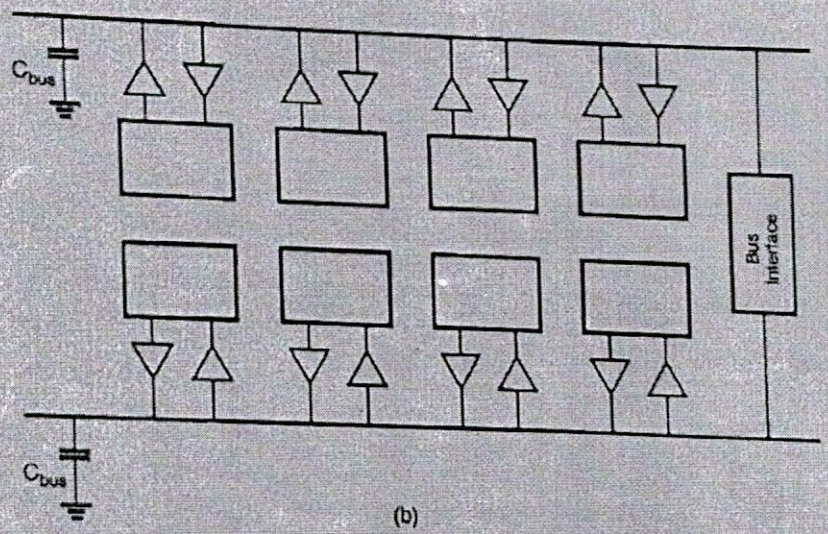


(a)



(b)

(a)Using a single global bus structure for connecting a large number of modules on chip results in large bus capacitance and large dynamic power dissipation.
(b) Using smaller local buses reduces the amount of switched capacitance, at the expense of additional chip area.

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