

BOARD OF STUDIES MEETING – 2022-23 K.S.R.M COLLEGE OF ENGINEERING

AUTONOMOUS

Minutes of the Meeting

Date	04.08.2022	Day	Thursday
Time	11.15AM	Venue	Online, Link: https://meet.google.com/sfs-asjf-ijf
Dept./SS	ECE	Convener	Dr. G. Hemalatha

Memb	persPresent:12			Meml	Members Absent: 01				
S.No	Name	Designation	Signature	S.No	Name	Designation			
	Prof. G. Hemalatha	Prof., & HOD ECE, KSRMCE	G. & h		Sri S. Guru Shankar	Director, Quality and Exports Chaitanya Chemicals Kadapa			
2.	Prof. P. Ramana Reddy	University nominee Professor in ECE, JNTUA Ananthapuramu							
3.	Prof. M. Rama Subba Reddy	Subject Expert Professor in ECE IIT Madras							
4	Dr. V. Anil Kumar	Subject Expert Asso.Prof.in ECE IIIT, Hyderabad							

5.	Sri S. P. Karthik	Principal Field Applications Engineer NI Systems (India) Pvt. Ltd. Bellandur, Bangalore			
6.	Prof. M.Venkatanarayana	Prof. in ECE, KSRMCE	MN.N.		
7.	Prof. V. Adinarayana Reddy	Prof. in ECE, KSRMCE	Mash pull)	
8.	Sri R.V. Sreehari	Asso. Prof., in ECE KSRMCE	A.		
9.	Dr. S. L. Prathapa Reddy	Asso. Prof., in ECE KSRMCE	s. I. nedly.		
10.	Dr. S. Zahiruddin	Asso. Prof., in ECE KSRMCE	Spenson ,		
11.	Sri Md. Mahaboob Pasha	Asso. Prof., in ECE KSRMCE	169P-7		
12.	Sri A. Valli Bhasha	Asst. Prof., in ECE KSRMCE	A.V. Bhash		

Dr. G. Hemalatha welcomed all the members to the meeting and presented the agenda of the meeting. The resolutions are:

	To do item	Discussion	Resolution	Coordinator/in- charge
1	semesters under R20 UG.	syllabus of V & VI semesters under R20UG. Including New Courses recommended Based on the Feedback given by the	"Digital signal Processing" in VI Semester R20UG. The committee suggested introducing "Software Defined Radio (SDR)" in R20	Prof. M. V. Narayana

Kadapa, Andhar Pardesh – 516003 www.ksrmce.ac.in

	premier institute syllabus.		
To approve the open elective courses and syllabus under R20UG.	The Head of the Department has presented the open elective courses and syllabus under R20UG.	The committee approved the open elective courses and syllabus under R20UG presented.	
and Minor degree courses and syllabus		The committee approved the Honor and Minor degree courses and syllabus under R20UG presented.	
and syllabus of I, II, III and IV semester under	presented the Curriculum and syllabus of I, II, III and IV	The committee suggested to Replace "Real Time operating systems" in the R22PG II semester with "Embedded and Real Time operating systems".	
Any other information for discussion.			-

The Head of the Department have proposed the Vote of thanks and concluded the meeting.

Convener

Professor & H.O.O.

Department of E.C.E. K.S.R.N. College of Engineering KADAPA - 818 093

Course Structure (R20) –III Year

				Sem	este	r-V	,		
S.No.	Code	Course Name	Category	L	T	P	IM	EM	Credits
1.	2004501	Embedded systems and IoT	ESC	3	0	0	40	60	3
2.	2004502	Communication Systems	PCC	3	0	0	40	60	3
3.	2004503	Antennas and Wave Propagation	PCC	3	0	0	40	60	3
	2004504	Professional Elective Course-I Electronic Measurements and Instrumentation	PEC	3	0	0	40	60	3
4.	2004505	Computer Architecture and Organization	PEC	3	0	0	40	60	3
	2004506	Optical Communication	PEC	3	0	0	40	60	3
5.		Job oriented or Open Elective course– I	OEC	2	0	2	40	60	3
6.	2004507	Communication Systems Lab	PCC	0	0	3	40	60	1.5
7.	2004508	Embedded systems and IoT lab	ESC	0	0	3	40	60	1.5
8.	20SC509	Introduction to Machine learning using Python (Skill oriented course – III)	SC	1	0	2	40	60	2
9.	20MC510	Management Organizational behavior	MC	3	0	0	40		0
10.	2004510	Community Service Project	PROJ				100		1.5
		Total							21.5

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAFA - 516 003

						Se	emester	-VI	
S.No	Code	Course Name	Category	L	T	P	IM	EM	Credits
1.	2004601	Digital Signal Processing(DSP)	PCC	3	0	0	40	60	3
2.	2004602	Microwave Engineering	PCC	3	0	0	40	60	3
3.	2004603	Control Systems	PCC	3	0	0	40	60	3
	2004604	Professional Elective Course - II CMOS VLSI Design	PEC	3	0	0	40	60	3
4.	2004605	Information Theory & Coding	PEC	3	0	0	40	60	3
	2004606	Sensors and Actuators	PEC	3	0	0	40	60	3
5.		Humanities Elective	HS	3	0	0	40	60	3
6.	2004607	DSP Lab	PCC	0	0	3	40	60	1.5
7.	2004608	Microwave & Optical Communication Lab	PCC	0	0	3	40	60	1.5
8.	2004609	VLSI Design Laboratory	PCC	0	0	3	40	60	1.5
9.	20SC610	Advanced English Communication lab (Skill Oriented Course – IV)	SC	1	0	2	40	60	2
10.	20MC509	Constitution of India	MC	2	0	0	40		0
		Total							21.5
		Industry Internship (N	Mandatory)	for 6	- 8 we	eks d	uration	during su	ımmer

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 083.

Course Title	Embedde o		tems a	B. Tech. ECE V Sem				
Course Code	Category	Hours/Week Credits			Maximum Marks			
2004501	ESC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3	0		3	40	60	100
Mid Exam Duration: 90Min					39-	End Exam	Duration	n: 3Hrs

- This course imparts knowledge on, introduction to IoT, its complete architecture & internet Protocols involved enabling IoT communication over the network.
- > The course also offers an introduction to IoT platforms, end devices, networks and cloud services.
- ➤ Using case analysis, assignments, Labs & projects students will acquire skills necessary to identify building blocks of an IoT application.

Course	Outcomes: On successful completion of this course, the students will be able to						
CO 1	Understanding of the communication protocols in IoT communications						
CO 2	Identify issues and design challenges in IoT applications.						
CO3	Describe the topologies and architectures of various processors and IoT						
CO 4	Apply appropriate hardware and software components for IoT applications.						
CO 5	Develop a models for IoT applications						

UNIT-I

Introduction to Embedded systems: Embedded system overview, features and architecture considerations-ROM, RAM, timers, data and address bus, Memory and I/O interfacing concepts, memory mapped I/O. CISC Vs RISC design philosophy, Von-Neumann Vs Harvard architecture.

UNIT-II

Introduction & Overview of Internet of things: Introduction to The Internet of things today, Vision of internet of things, An IoT architecture outline, Functional blocks of IoT, industrial IoT, Challenges in IOT, Hardware and Software tools required for IoT application development.

Case Study: Simple Link TM Wi-Fi ® Enabled Electronic Smart Lock.

UNIT-III

Internet/Web and Networking Basics: Introduction to internet & network topologies, TCP/IP protocol, TCP/IP Layers and their relative Protocols, IP addressing(IPV4), IP Address Classification & Subnet, Local IP, Gateway IP and DNS,TCP & UDP Communication, Overview of MAC Address, Energia Wi-Fi Library API's.

Case Study: Connected microcontrollers essential to automation in buildings.

UNIT-IV

MSP 432 processor: MSP 432 processor features, Architecture, its Booster Packs, Development Environment, Libraries, Fundamental Programming Concepts, TM4C123G Launchpad, Sensor hub Boosterpack, CC3220 SF Launchpad.

UNIT-V

Cloud Communication in IOT: IOT device to cloud storage communication Model, need of Cloud services in IOT, Different Cloud storage services, Cloud Data processing and frame format, Introduction to clouds like Temboo, Blynk, Pubnub etc.

IOT Platform and Application development: IoT applications in home, infrastructures, Healthcare, Transport, buildings, security, Industries, and other IoT electronic equipment, Adapting IPV6 for IOT Requirement(overview).

Text Books:

- 1. Internet of Things: Converging Technologies for Smart Environments and Integrate Ecosystems, Dr. OvidiuVermesan, Dr. Peter Friess, River Publishers.
- 2. Vijay Madisetti, ArshdeepBahga, "Internet of Things: A Hands-On Approach", Universities Press.

Reference Books:

- 1. Embedded Ethernet And Internet Complete (Designing and Programming Small Devices for Networking)by Jan Axelson.
- 2. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann.
- **3.** Mazidi, Muhammad Ali, "TI MSP432 ARM Programming for Embedded Systems (ARM books)" Volume 4, MicroDigitalEd, 2016.
- 4. K.V. Shibu, "Introduction to Embedded systems", Second edition McGrawHill Education.
 - 1. http://www.ti.com/ww/en/internet of things/iot-overview.html.
 - 2. http://energia.nu/reference/
 - 3. Internet of Things (IoT): A vision, architectural elements, and future directions JayavardhanaGubbia, RajkumarBuyyab, *, SlavenMarusic a, MarimuthuPalaniswami a
 - 4. http://www.ti.com/wireless-connectivity/simplelink-solutions/overview/overview.html.
 - 5. https://www.hivemq.com/blog/mqtt-essentials-part2-publish-subscribe.
 - 6. Cloud Computing Bible, Barrie Sosinsky, Wiley-India, 2010

Professor & H.O.O.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.

Course Cod	e Category	Hours	/Week		Credits	Maximum M	Iarks	
2004502	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
		3	0	0	3	40	60	100
Mid Exam I	Ouration: 90Min				End Exa	m Duration: 3	3Hrs	
Course Obj	ectives:							
•	To analyze differe	nt modu	lation ar	nd dem	odulation te	echniques.		
	To analyze variou	s transm	itter and	receiv	er functions	and circuits		
	To understand the					and circuits.		
	To understand the	HOISC III	Commu	meatio	11			
Course Oute	comes: On succes	sful com	pletion	of this	course the	students will h	e able to	
	Understand variou						c doic to	
CO 2	Apply basic princ						noise	
						on parameters,	HOISE	
	characteristics, entropy, channel capacity.							
CO 3	Analyze various modulators, demodulators, transmitters, receivers, Inter-symbol							

B. Tech. ECE V Sem

Communication Systems

Interference and error control techniques.

Design error control coding techniques

UNIT-I

CO 4

CO₅

Course Title

Introduction to communication systems: Modulation, its needs and types, Fundamental physical limitations.

Compare various modulation and demodulation techniques and signaling schemes.

Analog Modulation Schemes: AM, DSBSC and SSB- Generation and detection methods, FDM, Phase and frequency modulation, NBFM, WBFM, Multi-tone FM, Transmission band width of FM, direct and indirect generations of FM, Demodulation methods.

UNIT-II

Radio Transmitters and Receivers: Block diagram study of radio broadcast AM and FM transmitters, Super heterodyne AM and FM receivers, Measurement of sensitivity, selectivity, choice of IF, AGC.

Noise: External and internal sources of noise, Noise calculations, Noise equivalent resistant, Noise figure, Noise temperature, Effect of noise in AM and FM modulation system.

UNIT-III

Pulse Modulation: PAM generation and detection, PDM and PPM, Generation and detection. TDM, Comparison of TDM & FDM.

Waveform Coders: PCM system and its bandwidth requirement, Noise in PCM Systems, Quantization noise and SNR, Differential PCM, Delta modulation and Noise in delta modulation, Adaptive delta modulation.

UNIT-IV

Base band data transmission: Introduction, Inter-symbol Interference, Nyquist's Criterion for distortion less binary data, M-ary signaling scheme, Binary Vs M – ary, Eye diagrams.

Digital modulation schemes (Band Pass Data Transmission): Correlator and Matched filter receivers, ASK, FSK (coherent & Non Coherent), PSK, DPSK, Comparison of digital modulation schemes, M-ary signaling schemes- QPSK and QAM-case studies.

UNIT-V

Information theory: Introduction, Unit of information, Entropy, Rate of Information, Joint and conditional entropy, mutual information, channel capacity-Binary symmetric and non symmetric channels, Continuous Gaussian channel (Shannon- Hartley theorem)

Error control coding: Linear block codes- matrix description, Hamming codes, Decoding, Burst and random error correcting codes- Convolutional codes, code tree diagram, state diagram, trellis diagram.

Text Books:

- 1. Simon Haykin, "Communication Systems", Wileyestern, 1978, 4th edition.
- 2. Sam Shanmugam,, K "Analog & Digital Communication Systems", John Willey & Sons.

Reference Books:

- 1. R.P. Singh & S.D. Sapre, "Communication Systems, Analog & Digital", Tata McGraw-Hill
- **2.** B.P. Lathi, "Modern Digital and Analog Communication Systems", Oxford University Press, 2nd Edition, 1996.
- 3. Bernard Sklar, "Digital Communications", Prentice-Hall PTR, 2nd Edition, 2001.
- 4. Kennedy and Davis, "Electronic communication systems", 4thEdition, Mc Graw International edition, 1992.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003

Course Title			S AND AGATI	B. Tech. ECE V Sem				
Course Code	Category					Maximum Marks		
2004503	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
		3	0	0	3	40	60	100
Mid Exam Duration: 90Min					End Exa	m Duration:	3Hrs	

Course Objectives: The course should enable the students to:

- Be Proficient in the radiation phenomena associated with various types of antennas and understand basic terminology and concepts of antennas along with emphasis on their applications.
- Analyze the electric and magnetic field emission from various basic antennas with mathematical formulation of the analysis.
- Explain radiation mechanism of different types of antennas and their usage in real time field.
- Justify the propagation of the waves at different frequencies through different layers in the existing layered free space environment structure.

Course Ou	Course Outcomes: On successful completion of this course, the students will be able to						
CO 303.1	Define various antenna parameters						
CO 303.2	Describe the radiation mechanisms of various antennas.						
CO 303.3	Analyze characteristics of antenna arrays.						
CO 303.4	Calculate Various parameters of antenna.						
CO 303.5	Analyze the effects of atmosphere on wave propagation.						

UNIT-I

Antenna Basics: Introduction, Basic antenna parameters- patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity-Gain-Resolution, Effective height, Antenna Apertures, Friis transmission formula, Illustrative problems. Fields from oscillating dipole, Antenna temperature, front—to-back ratio, basic Maxwell's equations, retarded potential-Helmholtz Theorem, Radiation from Small Electric Dipole, Quarter wave Monopole and Half wave Dipole—Current Distributions, Field Components, Radiated power, Radiation Resistance, Beam width, Directivity, Effective Area and Effective Height, Natural current distributions, far fields.

UNIT-II

Antenna Arrays: Point sources- Definition, Patterns, arrays of 2 Isotropic sources. Principle of Pattern Multiplication, Uniform Linear Arrays – Broadside Arrays, End fire Arrays, Derivation of their characteristics and comparison, BSA with Non-uniform Amplitude Distributions, Binomial Arrays.

UNIT-III

VHF, UHF AND Microwave Antennas: Arrays with Parasitic Elements, Yagi - Uda Arrays,

Folded Dipoles & their characteristics. Helical Antennas, Horn Antennas, Parabolic Reflector, Micro strip Antennas. Antenna Measurements: Introduction, Directivity Measurement, Gain Measurements (by comparison, Absolute and 3-Antenna Methods), case study.

UNIT-IV

Wave Propagation-I: Introduction, Characterizations and general classifications, different modes of wave propagation, Ray/ Mode concepts. Ground wave propagation - Introduction, Plane earth reflections, Space and surface waves, wave tilt, curved earth reflections. Space wave propagation- Introduction, field strength variation with distance and height, effect of earth's curvature, absorption, Super refraction, M-curves and duct propagation, scattering phenomena, tropospheric propagation, fading and path loss calculations.

UNIT-V

Wave Propagation-II: Sky wave propagation- Introduction, structure of Ionosphere, refraction and reflection of sky waves by Ionosphere, Ray path, Critical frequency, MUF, LUF, OF, Virtual height and Skip distance, Relation between MUF and Skip distance, Multi-HOP propagation, Energy loss in Ionosphere, Summary of Wave Characteristics in different frequency ranges.

Text Books:

- 1. John D. Kraus, Ronald J. Marhefka and Ahmad S. Khan, "Antennas and wave propagation", TMH, New Delhi, 4th Edition, (Special Indian Edition), 2010
- 2. E.C. Jordan and Balmain, "Electromagnetic Waves and Radiating Systems", PHI, 2nd Edition, 2000.
- 3. C.A. Balanis, "Antenna Theory" John Wiley & Sons, 2nd Edition, 2001.

Reference Books:

- 1. K.D. Prasad, "Antennas and Wave Propagation", Satya Prakashan, Tech India Publications, New Delhi, 2001.
- 2. F.E. Terman, "Electronic and Radio Engineering," McGraw-Hill, 4 th Edition, 1955.
- 3. Warren L. Stutzman, Gary A. Thiele, "Antenna Theory and Design", John Wiley & Sons, 3rd Edition.
- 4. Richard C. Johnson, "Antenna Engineering Handbook", McGraw-Hill, 1993.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093.

Course Title	ELECTRO I		MEASUI JMENT			B. Tech. EC	B. Tech. ECE V Sem Maximum Marks		
Course Code	Category	Hou	rs/Week		Credits	Maximum M	Iarks		
2004504	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total	
		3	-		3	40	60	100	
Mid Exam Du	ration: 90Mir	1				End Exam	Duratio	n· 3Hrs	

- · To know various measuring systems and their functionality.
- To understand various measurement metrics for performance analysis.
- To explain principles of operation and working of different electronic instruments.
- To familiarize the characteristics, operations, calibrations and applications of the different Oscilloscopes.
- To provide exposure to different sensors and transducers.

	1								
Course	ourse Outcomes: On successful completion of this course, the students will be able to								
CO 1	Understand the principle of operation of various Analog Instruments, Digital Instruments,								
	CROs, Bridges and transducers.								
CO 2	Describe the working f various analog and digital instruments.								
CO 3	Compare the various Analog Instruments, Digital Instruments, CROs, Bridges and								
	transducers.								
CO 4	Apply the various Analog Instruments, Digital Instruments, CROs, Bridges and								
	transducers in measurements.								

UNIT-I

Performance characteristics of Instruments: Static characteristics- Accuracy, Resolution, Precision, Expected value, Error, Sensitivity. Errors in Measurement. Dynamic Characteristics-Speed of response, Fidelity, Lag and Dynamic error.

Analog Instruments: Transistor Voltmeter, Micro Voltmeter (Chopper type) – DC Differential voltmeter – AC voltmeters – Multi meter -wave analyzers (AF & RF) – Harmonic distortion analyzer-Spectrum analyzer-Applications.

UNIT-II

Digital Instruments: Digital Voltmeters (Ramp, Dual slope, stair case, successive approximation types) Digital multi meter, Universal counter, Digital tachometer, Digital Phase meter.

UNIT-III

Cathode Ray Oscilloscopes: Motion of electron in electronic field and in magnetic field-Block diagram of CRO, CRT, Electrostatic deflection sensitivity – Vertical and Horizontal deflection systems – Principle of operation of dual beam, dual trace, sampling and storage CRO"s.

UNIT-IV

Bridges: Wheat stone bridge, Kelvin Bridge, Measurement of inductance- Maxwell's bridge, Anderson Bridge. Measurement of capacitance -Schering Bridge, Wien Bridge Errors and precautions in using bridges- Q meter and measurement methods

UNIT-V

Transducers: Active & passive transducers, Resistance, Capacitance, inductance; Strain gauges, LVDT, Piezo Electric transducers, Resistance Thermometers, Thermocouples, Thermistors, Sensistors.

Measurement of physical parameters - Force, Pressure, Velocity, Humidity, Moisture, Speed, Proximity and Displacement. Data Acquisition Systems.

Text Books:

- 1. H.S. Kalsi, "Electronic instrumentation", second edition, Tata McGraw Hill, 2004.
- 2. A.D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measurement Techniques", 5th Edition, PHI, 2002.

Reference Books:

- 1. Ernest O. Doebelin and Dhanesh N Manik, "Measurement Systems", 6th Ed., TMH,2010
- 2. David A. Bell, "Electronic Instrumentation & Measurements", 2nd Edition, PHI, 2003.
- 3. Robert A.Witte, "Electronic Test Instruments, Analog and Digital Measurements", 2nd Ed., Pearson Education, 2004.
- 4. K. Lal Kishore, "Electronic Measurements & Instrumentations", Pearson Education 2005

Professor & H.O.O.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093

Course Title	COMPU		RCHITI NIZAT		E AND	B. Tech. ECl	Hind		
Course Code	Category	Но	Hours/Week Credits			Maxi	mum Ma	rks	
2004505	PCC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total	
		3	-	'	3	40	60	100	
Mid Exam Duration: 90Min						End Exam	Duration	ı: 3Hrs	

- To understand the architecture of a modern computer with its various processing units. Also the Performance measurement of the computer system.
- To understand the memory management system of computer.
- To understand the various instructions, addressing modes.
- To understand the concept of I/O organization.

Course	ourse Outcomes: On successful completion of this course, the students will be able to							
CO 1	Understand the architecture of modern computer, different instruction types, concepts of I/O Organization and Memory systems.							
CO 2	Analyze the Performance of a computer using performance equation, Instruction Sequencing, Input/output Operations							
CO 3	Describe Addressing Modes, Buses memory circuits, Micro programmed Control and Execution of Complete Instruction							
CO 4	Compare the buses and memory systems.							

UNIT-I

Basic Structure Of Computers: Functional unit, Basic Operational concepts, Bus structures, System Software, Performance, The history of computer development.

Machine Instruction and Programs: Instruction and Instruction Sequencing, Register Transfer Notation, Assembly Language Notation, Basic Instruction Types.

UNIT-II

Central Processing Unit: General registers Organization, Stack Organization, Instruction formats, Addressing Modes, Program Control, RISC, Parallel Processing, Pipelining, Arithmetic Pipeline, and Instruction Pipeline.

Type of Instructions: Arithmetic and Logic Instructions, Branch Instructions, Addressing Modes, Input/output Operations

UNIT-III

Input/Output Organization: Accessing I/O Devices, Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access.

Buses: Synchronous Bus, Asynchronous Bus, Interface Circuits, Standard I/O Interface: Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB).

UNIT-IV

The Memory Systems: Basic memory circuits, Memory System Consideration, Read Only Memory: ROM, PROM, EPROM, EEPROM, Flash Memory, Cache Memories: Mapping Functions, INTERLEAVING

Secondary Storage: Magnetic Hard Disks, Optical Disks,

UNIT-V

Processing Unit: Fundamental Concepts: Register Transfers, Performing an Arithmetic Or Logic Operation, Fetching A Word From Memory, Execution of Complete Instruction, Hardwired Control, Micro programmed Control- Microinstructions, Micro program Sequencing, Wide Branch Addressing Microinstructions with next—Address Field

Text Books:

- 1. Carl Hamacher, Zvonks Vranesic, SafeaZaky "Computer Organization", McGraw Hill, 5thEdition2011.
- 2. John P. Hayes "Computer Architecture and Organization", McGrawHill,3rdEdition, 2002.

Reference Books:

- 1. William Stallings "Computer Organization and Architecture "- Pearson/PHI, Sixth Edition,
- 2. Andrew S. Tanenbaum "Structured Computer Organization" PHI/Pearson, 4th Edition2012.
- 3. Sivaraama Dandamudi "Fundamentals of Computer Organization and Design", Springer Int.Edition, 2003. J.P. Hayes, "Computer Architecture and Organization", McGraw-H

Professor & M.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093.

Course Title	OPTIC	AL CO	MMUN	ICAT	ION	B. Tech. EC	E V Sem	
Course Code	Category	H	Hours/Week			Maxin	num Mar	ks
2004506	PEC L T P C Continu	Continuous Internal Assessment	End Exams	Total				
		3	-	-	3	40	60	100
Mid Exam Dur	ation: 90Min					End Exam	Duratio	n: 3Hrs

- To understand the functionality of various components of fiber optical fiber communication system.
- To understand the properties and principles of different types of optical fibers, and losses that occur in fibers.
- To understand the working principle of optical sources (LED and LASER) and power launching schemes.
- To analyze the operation of various optical detectors (PIN & APD) and optical receiver.
- To understand the design of optical systems, WDM and Measurements.

	and the desirence of the state						
Course	Outcomes: On successful completion of this course, the students will be able to						
CO 1	Understand the structures of Optical fibers based on modes, refractive index and fiber						
	materials, principle of Optical Sources and detectors.						
CO 2	Describe Transmission Characteristics of optical fibers, Rays & Modes in Optical Fiber,						
	fiber Power Launching, Joints and splicing.						
CO3	Compare the types of optical sources and optical detectors on the basis of construction						
	and principle of operation.						
CO 4	Analyze the different kind of losses and dispersions in fibers, parameters in Optical						
	system design.						
CO 5	Evaluate various parameters in designing Optical receivers.						

UNIT-I

Introduction to Optical fibers: Historical Development, General communication System, Optical Fiber Communication System, Advantages & Applications of Optical Fiber Communication, Ray Theory transmission, Total Internal Reflection, Acceptance angle, Numerical Aperture, Rays & Modes in Optical Fiber, V-Number, Mode coupling, Cylindrical Fiber- Step Index & Graded Index Fibers, Single & Multi mode fibers, Cut off wavelength, Mode Field Diameter, Effective Refractive Index, Simple problems.

UNIT-II

Fiber Materials: Glass fibers, Halide glass fibers, Active glass fibers, Chalgenide glass fibers, Plastic optical fibers, Mechanical Properties of Fibers, Fiber Optic Cables.

Transmission Characteristics of optical fibers: Attenuation, Losses in optical fiber-Absorption Losses, Scattering Losses, Bending Losses, Core and Cladding losses, Dispersion-Chromatic dispersion, Material dispersion, Wave guide dispersion, Polarization Mode Dispersion, Intermodal dispersion, Fiber Birefringence

UNIT-III

Optical Sources: Introduction, Light Emitting Diodes (LEDs), LED Structures-Surface Emitting LED & Edge emitting LED, Light Source Materials, Quantum efficiency and LED Power, Modulation of LED, Advantages of LED, LASER Diodes, Laser action processes, Laser Diode Modes and Threshold Conditions, Laser Diode Rate Equations, External Quantum Efficiency, Resonant Frequencies, Advantages of LASER Diode, Comparison of LED & LASER Diodes.

Photo Detectors: Requirements of photo detectors, PIN photo detector, Avalanche photo diode (APD), Detector response time, Structures for InGaAs APDs, Temperature effect on avalanche gain, comparisons of photo detectors, case studies.

UNIT-IV

Power launching and Coupling: Introduction, Source to Fiber Power Launching, Source output pattern, power coupling calculation, power launching versus wavelength, Equilibrium Numerical Aperture, Lensing schemes for Coupling Improvement, Non imaging microsphere, Laser diode to fiber coupling, LED coupling to single mode fibers.

Fiber to fiber Joints-Mechanical misalignment, Fiber Splicing-Splicing techniques, splicing single mode fibers, Optical Fiber Connectors-Connector types, Single mode fiber connectors-Connector return losses, Passive components-2 x 2 fiber coupler, Star couplers.

UNIT-V

Optical receiver operation: Fundamental receiver operation, Digital signal transmission, error sources, Receiver configuration, Optical system design-Point to point links, system considerations, Link Power budget, Rise time budget, Transmission distance, Concept of WDM-Operational principle, Types, Fiber grating filters. Measurements-Optical Time domain Reflectometer (OTDR), Attenuation Measurements-Cut back technique & Insertion loss method, Dispersion Measurements, EYE Patterns.

Text Books:

- 1. Gerd Keiser, "Optical fiber communications", McGraw Hill International Edition, 4th Edition, 2010.
- 2. John M. Senior, "Optical fiber communications", Prentice Hall of India, 3rd Edition, 2010.

Reference Books:

- 1. Max Ming-Kang Liu, "Principles and Applications of Optical Communications", TMH, 2010.
- 2. S. C. Gupta, "Text book on optical fiber communication and its applications", Prentice Hall of India, 2005.
- 3. Satish Kumar, "Fundamentals of Optical Fiber communications", Prentice Hall of India, 2009.

Professor & M.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.

Course	Title	Comr	nunicat	ion Syst	ems La	b	B. Tech. EC	E V Sem		
Course	Code	Category	Но	ours/We	ek	Credits		ıum Mar	ks	
2004:	2004507 PC		L	Т	P	C	Continuous Internal Assessment	End Exams	Total	
			-	-	3	1.5	40	60	100	
							End Exam	Duration	n: 3Hrs	
Course	•									
• [Design a	nd generation of	of AM, I	PM, FM,	ASK,P	SK, QPSK	communication	n techniq	ues.	
• [Jsage of	Communication	ons test	equipme	nt.			i e		
Course	Outcon	ies: On success	ful com	pletion o	of this c	ourse, the	students will be	e able to		
CO 1	Apply	the knowledge	of Amp	olitude, I	requen	cy and Pul	se Modulation	Systems	in	
		he knowledge of Amplitude, Frequency and Pulse Modulation Systems in ing analog Communication systems.								
CO 2		the knowledg				Modulatio	n FSK PSK I	DPSK OP	SK in	
		ping Digital Co				Wiodulatio	ii, 1 5ix, 1 5ix, 1	or six,Qr	SK III	
CO 3					25.4		D' 1 11			
CUS		n measuremen		ensitivity	y, Select	tivity and I	Fidelity of Con	nmunicati	on	
	Charles Carles March 11	tems and syster	20m - 10m -							
CO 4	Test ec	quipment to test	variou	s commi	unicatio	n systems	they develop			
CO5	Apply	the knowledge	of Amp	olitude, I	requen	cy and Pul	se Modulation	Systems	in	
		ping analog Co						Jerenio		

Part- A: Analog Communication Lab:

- 1. Amplitude modulation and demodulation.
- 2. Frequency modulation and demodulation.
- 3. Characteristics of Mixer.
- 4. Pre-emphasis & de-emphasis.
- 5. Pulse Amplitude Modulation and demodulation.
- 6. Pulse Width Modulation and demodulation.
- 7. Pulse Position Modulation and demodulation.
- 8. Radio Receiver measurements Sensitivity, Selectivity, & Fidelity.

Part- B: Digital Communication Lab:

- 1. Sampling Theorem verification.
- 2. Time division multiplexing.
- 3. Pulse Code Modulation.
- 4. Delta modulation.
- 5. Frequency shift keying Modulation and Demodulation.
- 6. Phase shift keying Modulation and Demodulation.
- 7. Differential phase shift keying Modulation and Demodulation.
- 8. QPSK Modulation and Demodulation

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093

Course Title	Embedde	d Sys	tems a	nd Id	T Lab	B. Tech. ECE V Sem		
Course Code	Category	Н	ours/We	eek	Credits	Maximum Marks		
2004508	ESC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
			0	3	1.5	40	60	100
						End Exam	Duration	n: 3Hrs

- This course imparts knowledge on, Arduino Uno, Raspberry pi, MSP430F5529LP and TM4c123G Launch pad.
- > The course also offers an introduction to IoT platforms, end devices and cloud services.
- ➤ Using these fundamentals learnt in the Lab, students can do projects and will acquire skills necessary to implement an IoT application.

Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	CO 1 Understand and Identify issues and design challenges in IoT applications.						
CO 2	Select appropriate hardware and software components for IoT applications.						
CO 3	Conceptual knowledge will help students to build IoT projects.						
CO 4	Understanding of the communication protocols in IoT communications						
CO 5	Familiarize with application program interfaces for IoT						

Hardware required: MSP430F5529LP, Arduino Uno, Raspberry pi, TM4C123G Launch pad, Sensor hub Booster pack, CC3220 SF Launch pad.

Software required: Energia v17, Code Composer studio, Arduino Uno, Raspbian, CC3100 SDK, CC3220 SDK & a Serial terminal software.

Lab 1.

- a) Program the MSP430 for Led blink, switch usage, ADC, PWM generation & serial communication.
- b) Write a program by using WiFi libraries, to connect your Launchpad with the available Encrypted/non-encrypted WiFi network.

Lab 2.

- a) Write a program to connect the launch pad with WiFi & print IPAddress, GatewayIP, Subnetmask on Serial Monitor.
- b) Write a program to assign a static IP, Gateway & Subnet to a WiFi Connected controller.

Lab 3.

- a) Design a Client server model between two WiFi modules and establish the communication between the two.
- b) Write a program to design client server model based on TCP & UDP communication Protocols.

Lab 4.

Design a HTTP based web server to manipulate the GPIO's of WiFi Module and monitor Sensor data connected with WiFi Module.

Lab 5.

Use Blynk API's and write a program to control your Launchpad with Mobile Application.

Lab 6.

Using temboo credentials connect your launchpad with Yahoo weather to receive weather details in serial terminal.

Lab 7.

With the help of Temboo services, generate Code for CC3220SF launchpad and upload it from TI CCS Cloud.

Lab 8.

Design a Simple MQTT Based communication model to retrieve sensor data from a cloud Storage.

Lab 9.

Getting started with WLAN Access point & Station using CC3100SDK using CCS and SimplinkWiFi Library.

Lab 10.

Import and execute Email Send Application using CC3100 SDK in CCS and understand Simplink API usage.

Note: Use either MSP430, Arduino or Raspberry pi Launch pad to perform the above experiments.

ADDITIONAL EXPERIMENTS

- Traffic light control interfacing
- Stepper motor control interfacing

Note: Use either MSP430, Arduino or Raspberry pi Launch pad to perform the above experiments.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 063.

Course Title	Introduction		achine I ython	Learnin	g using	B. Tech. ECE V Sem		
Course Code	Category	He	ours/We	eek	Credits	Maximum Marks		
20SC509	SC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		1	-	2	2	40	60	100
						End Evam	Duration	n. 3Hre

- To create awareness on machine learning
- To know step by step procedure to run ML model
- To differentiate the supervised and unsupervised algorithms
- · To know the architecture of ANN and CNN.

	0.111						
Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	Understand fundamentals of Machine Learning						
CO 2	Analyze flow chart to build a Machine Learning model						
CO 3	Apply concepts of Machine learning in real time						
CO 4	Develop ANN and CNN models for real time applications						

UNIT-I

The Fundamentals of Machine Learning: Introduction, Types of Machine Learning Systems-Supervised/Unsupervised Learning, Batch and Online Learning, Instance-Based Versus Model-Based Learning; Main Challenges of Machine Learning-Insufficient Quantity of Training Data, Non representative Training Data, Poor-Quality Data, Irrelevant Features, Over fitting the Training Data, Under-fitting the Training Data, Stepping Back, Testing and Validating.

UNIT-II

End-to-End Machine Learning Project: Working with Real Data, Look at the Big Picture-Frame the Problem, Select a Performance Measure, Check the Assumptions, Get the Data-Create the Workspace, Download the Data, Take a Quick Look at the Data Structure, Create a Test Set, Discover and Visualize the Data to Gain Insights-Visualizing Geographical Data, Looking for Correlations, Experimenting with Attribute Combinations, Prepare the Data for Machine Learning Algorithms-Data Cleaning, Handling Text and Categorical Attributes, Custom Transformers, Feature Scaling, Transformation Pipelines, Select and Train a Model.

UNIT-III

Classification: Training a Binary Classifier, Performance Measures-Measuring Accuracy Using Cross-Validation, Confusion Matrix, Precision and Recall, Precision/Recall Tradeoff, The ROC Curve; Multiclass Classification, Error Analysis, Multi label Classification, Multi output Classification,

Training Models: Linear Regression, The Normal Equation, Computational Complexity, Gradient Descent-Batch Gradient Descent, Stochastic Gradient Descent, Mini-batch Gradient Descent; Polynomial Regression, Learning Curves, Regularized Linear Models, Ridge Regression, Lasso Regression, Elastic Net ,Early Stopping; Logistic Regression-Estimating

Probabilities, Training and Cost Function, Decision Boundaries, Softmax Regression.

UNIT-IV

Support Vector Machines: Linear SVM Classification-Soft Margin Classification, Nonlinear SVM Classification-Polynomial Kernel, Adding Similarity Features, Gaussian RBF Kernel, and Computational Complexity

Dimensionality Reduction: The Curse of Dimensionality, Main Approaches for Dimensionality Reduction-Projection, Manifold Learning; PCA- Preserving the Variance, Principal Components, Projecting Down to d Dimensions, Using Scikit-Learn, Explained Variance Ratio, Choosing the Right Number of Dimensions, PCA for Compression, Incremental PCA, Randomized PCA, Kernel PCA.

UNIT-V

Introduction to Artificial Neural Networks: From Biological to Artificial Neurons, Biological Neurons, Logical Computations with Neurons, The Perceptron, Multi-Layer Perceptron and Back propagation; Training an MLP with Tensor Flow's High-Level API, Training a DNN Using Plain Tensor Flow -Construction Phase, Execution Phase Using the Neural Network, Fine-Tuning Neural Network Hyper parameters, Number of Hidden Layers, Number of Neurons per Hidden Layer, Activation Functions

Convolutional Neural Networks : The Architecture of the Visual Cortex, Convolutional Layer Filters, Stacking Multiple Feature Maps, Tensor Flow Implementation, Memory Requirements Pooling Layer, CNN Architectures, LeNet-5, Alex Net, GoogLe Net and Res Net.

Text Books:

- 1. Aurélien Géron, "Hands-On Machine Learning with Scikit-Learn and TensorFlow Concepts, Tools, and Techniques to Build Intelligent Systems", O'reilly publishers, 2017
- 2. Chris albon, "Machine Learning with Python cookbook", O'reilly publishers, 2018

Reference Books:

- 1. Oliver Theobald, "Machine Learning For Absolute Beginners", A Plain English Introduction (2nd Edition)
- 2. John Paul Mueller and Luca Massaron, "Machine Learning (in Python and R) For Dummies" (1st Edition)

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093.

Course Title	MANAGEM I		ORGA IOR (N		ΓΙΟΝΑL	B. Tech. EC	E V Sem	
Course Code	Category	H	ours/We	eek	Credits	Maxin	ıum Mar	ks
20MC510	MC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3			-	40	-	40
Mid Exam Dur	Mid Exam Duration: 90Min					End Exam	Duration	n: -

Course Objectives: The main objective of the course is to learn

- · To aid students in understanding human behavior in organizations,
- To provide students with a comprehensive exposure to organizational behavior theories, research and workplace issues.
- The course also provides an overview of the theories and practices of management in organizational contexts.

Course	Course Outcomes: On successful completion of this course, the students will be able to							
CO 1	Explain the Importance & Role of Management in the Organizations.							
CO 2	Evaluate the different aspects related to Decision Making and Controlling Process							
CO 3	Describe the different theories related to Individual behavior in the Organization							
CO 4	Analyze Group Behavioral influence in the Organization.							
CO 5	Evaluate the process and climate effects in Organization Behavior.							

UNIT-I

Role of Management:

Concept – Significance – Functions – Principles of Management - Patterns of Management: Scientific – Behavioural – Systems – Contingency.

UNIT-II

Decision Making & Controlling – Process – Techniques. Planning – Process – Problems — Making It Effective. Controlling - System of Controlling – Controlling Techniques – Making Controlling Effective

UNIT-III

Individual Behaviour& Motivation – Understanding Individual Behaviour – Perception – Learning – Personality Types – Johari window- Transactional Analysis- Motivation – Concept of Motivation - Motivational Theories of Maslow, Herzberg, David McClelland, and Porter and Lawler

UNIT-IV

Group Behavior & Leadership: Benefits of Groups – Types of Groups – Group Formation and Development. Leadership and Organizational Culture and Climate: Leadership – Traits Theory – Managerial Grid – Transactional Vs Transformational Leadership – Qualities of good leader-Women Leadership in India.

UNIT-V

OrganisationalBehaviour: Organizing Process – Departmentation Types – Making Organizing Effective – Organisational culture- Types of culture – Organisational Culture VsOrganisational climate - Conflict management - Change Management

Textbooks:

- 1. Organisational Behaviour, Stephen P. Robbins, Pearson Education
- 2. Management and Organisational Behaviour, Subbarao P, Himalaya Publishing House
- 3. Principles of Management, Koonz, Weihrich and Aryasri, Tata McGraw Hill.

References:

- 1. Organisational Behaviour ,S.S.Khanka, S.Chand
- 2. Organisational Behaviour, Mishra .M.N, Vikas
- 3. Management and Organisationalbehaviour, Pierce Gordner, Cengage.
- 4. Behaviour in Organizations, Hiriyappa .B.New Age Publications
- 5. Organisational Behaviour, Sarma, Jaico Publications.
- 6. Principles of Management , Murugesan , Laxmi Publications

Professor & M.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 063.

Course Title	DIGITA	L SIGN	IAL PR	SING	B. Tech. EC	E VI Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2004601	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Duration: 90Min						End Exam	Duration	n: 3Hrs

- To become familiar with Discrete Fourier Transform and its efficient computation.
- To understand various IIR and FIR realization techniques.
- To know the design of IIR and FIR filters.

Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	Apply FFT to compute DFT and IDFT, Various transformation techniques and						
	Windows in designing digital filters, Decimation and Interpolation in the development						
	of Multirate systems.						
CO 2	Realize Various Digital Filters.						
CO 3	Solve problems related to IIR and FIR filters, sampling rate conversion.						
CO 4	Design IIR filters, FIR filters, Decimator and Interpolator.						

UNIT-I

Discrete Fourier series: DFS representation of periodic sequences, Properties of discrete Fourier series, Discrete Fourier Transform (DFT), properties of DFT, linear convolution of sequences using DFT.

Fast Fourier Transforms: Efficient computation of the DFT, Decimation in time and decimation in frequency FFT algorithms, FFT algorithms for composite N.

UNIT-II

Realization of Digital Filters: Block diagram representation of linear constant-coefficient difference equations, basic structures of IIR filters- direct form I, direct form II, transposed form, cascade form, parallel forms, basic structures of FIR filters-Direct form, Cascade form, Linear phase structure, Lattice structures.

UNIT-III

IIR Digital Filters: General considerations-Causality and its implications, Characteristics of Practical Frequency-selective filters, Design of analog filters-Butterworth and chebyshev approximations, IIR filter design by backward difference, Impulse Invariance, Bilinear transformation, design examples: frequency transformations, Illustrative Problems.

UNIT-IV

FIR Digital Filters: Symmetric and Anti-symmetric FIR filters, Design of Linear Phase FIR digital filters using windows, Frequency sampling technique, comparison of IIR and FIR filters, Illustrative Problems, applications of DSP (Dual Tone Multifrequency signal detection, Spectral analysis of sinusoidal and non-stationary signals).

UNIT-V

Multirate Signal Processing: Review of sampling, Introduction to Multirate sampling, Decimation, and interpolation, Sampling rate conversion by a rational factor, Multistage implementation of sampling rate conversion, Applications of multirate signal processing.

Text Books:

- 1. A.V. Oppenheim and R.W. Schaffer, & J R Buck, "Discrete Time Signal Processing," 2nd ed., Pearson Education, 2012.
- 2. John G. Proakis, Dimitris G. Manolakis, "Digital signal processing, principles, Algorithms and Aapplications", Pearson Education/PHI, 4th Edition, 2007.
- 3. Sanjit K Mitra, "Digital signal processing", A computer base approach- Tata McGraw-Hill, 3rd Edition, 2009.

Reference Books:

- 1. Andreas Antoniou, Digital signal processing: Tata McGraw-Hill, 2006.
- 2. Digital signal processing: M H Hayes, Schaum's Outlines, Tata McGraw-Hill, 2007.
- 3. A. Anand Kumar, "Digital Signal Processing," PHI Learning, 2011.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 063

Course Title	MICRO	WAVI	E ENGI	ING	B. Tech. EC	E VI Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2004602	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
		3	-		3	40	60	100
Mid Exam Duration: 90Min						End Exam	Duratio	n: 3Hrs

- To get familiarized with microwave frequency bands, their applications and to understand the limitations and losses of conventional tubes at these frequencies.
- To impart Knowledge about various microwave components, microwave junctions, microwave tubes and microwave signal characteristic measurements.
- To impart the knowledge of Scattering Matrix, its formulation and utility, and establish the S Matrix for various types of microwave junctions.

Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	List applications of microwaves and state principles of various microwave devices (L1)						
CO 2	Explain principle and working of microwave tubes and semiconductor devices (L2)						
CO 3	Describe fabrication of Microstrip lines; Microwave bench setup for various microwave measurements (L2)						
CO 4	Determine S – parameters of various microwave devices (L3)						
CO 5	Compute microwave signal parameters, power output and efficiency of microwave active devices (L4)						

UNIT-I

Microwave Transmission Lines: Introduction, Microwave Spectrum and Bands, Applications of Microwaves. Rectangular Waveguides – TE/TM modes, Expressions for Fields, Characteristic Equation and Cut-off Frequencies, Filter Characteristics, Dominant and Degenerate Modes, Sketches of TE and TM mode fields in the cross-section, Mode Characteristics – Phase and Group Velocities, Wavelengths and Impedance Relations, Impossibility of TEM mode. Related Problems.

Microstrip Lines: Introduction, Characteristic Impedance of Microstrip lines, Zo Relations, Effective Dielectric Constant, Losses.

UNIT-II

Microwave Tubes: Limitations and Losses of conventional tubes at microwave frequencies, Reentrant Cavities, Microwave tubes – O type and M type classifications, Otype tubes :2 Cavity Klystrons – Structure, Velocity Modulation Process and Applegate Diagram, Bunching Process and Small Signal Theory –, Applications, Reflex Klystrons – Structure, Applegate Diagram and Principle of working, Electronic Admittance; Oscillating Modes and output Characteristics, Electronic and Mechanical Tuning, Applications,

UNIT-III

Helix TWTs: Significance, Types and Characteristics of Slow Wave Structures; Structure of TWT and Suppression of Oscillations.

M-type Tubes: Introduction, Cross-field effects, Magnetrons – Different Types, 8-Cavity Cylindrical Travelling Wave Magnetron – Hull Cut-off Condition, Modes of Resonance and PI-Mode Operation, Separation of PI-Mode, o/p characteristics.

UNIT-IV

Waveguide Components and Applications: Coupling Mechanisms – Probe, Loop, Aperture types. Waveguide Discontinuities – Waveguide irises, Tuning Screws and Posts, Matched Loads. Waveguide Attenuators – Resistive Card, Rotary Vane types; Waveguide Phase Shifters – Dielectric, Rotary Vane types, Scattering Matrix—Significance, Formulation and Properties, S-Matrix Calculations for – 2 port Junction, E-plane and H-plane Tees, Magic Tee, Hybrid Ring; Directional Couplers – 2Hole, Bethe Hole types, Ferrite Components— Faraday Rotation, Gyrator, Isolator, Circulator and case studies.

UNIT-V

Microwave Solid State Devices: Introduction, Classification, Applications. TEDs – Introduction, Gunn Diode – Principle, RWH Theory, Characteristics, Basic Modes of Operation, Oscillation Modes, IMPATT Diode, Varactor Diode, case studies.

Microwave Measurements: Description of Microwave Bench – Different Blocks and their Features, Precautions; Microwave Power Measurement – Bolometer Method. Measurement of Attenuation, Frequency, Q- factor, Phase shift, VSWR, Impedance Measurement

Text Books:

- 1. Samuel Y. Liao, 'Microwave Devices and Circuits,' PHI, 3rd Edition, 2003.
- 2. Annapurna Das and Sisir K.Das, 'Microwave Engineering,' McGraw Hill Education, 3rd Edition, 2017.

Reference Books:

- 1. R.E. Collin, 'Foundations for Microwave Engineering,' John Wiley, 2nd Edition, 2007.
- 2. M.Kulkarni, 'Microwave and Radar Engineering,'Umesh Publications, 4th Edition, 2012
- 3. George Kennedy, 'Electronic Communication System,'McGrawHill, 6th Ed., 2017.
- 4. David M. Pozar, 'Microwave Engineering, An Indian Adaptation: Theory and Techniques,' Wiley, 2020.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.

Course Title	CONTROL SYSTEMS					B. Tech. EC	E VI Sem	
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2004603	PCC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3	-		3	40	60	100
Mid Exam Duration: 90mins						End Exam	Duratio	n: 3Hrs

- To learn Merits and demerits of open loop and closed loop systems; the effect of feedback
- The use of block diagram algebra and Mason's gain formula to find the overall transfer function
- To learn Transient and steady state response, time domain specifications and the concept of Root loci.
- To learn Frequency domain specifications, Bode diagrams and Nyquist plots
- To learn State space modeling of Control system

	to rear state space moderning of control system							
Course	Course Outcomes: On successful completion of this course, the students will be able to							
CO 1	Understand the concepts of control systems classification, feedback effect, mathematical							
	modeling, time response and frequency response characteristics, state space analysis							
CO 2	Analyze time response analysis, error constants, and stability characteristics of a given							
	mathematical model using different methods							
CO 3	Apply various criteria to test the stability of a given system.							
CO 4	Design and develop different compensators, controllers and their performance evaluation for							
	various conditions. Implement them in solving various engineering applications							

UNIT-I

Control System Concepts: Open loop and closed loop control systems and their differences-Examples of control systems-classification, transfer function, effect of feedback, mathematical modeling of physical systems, block diagram, reduction techniques, signal flow graphs and mason's gain formula.

UNIT-II

Time Domain Analysis: Standard test signals, time response of first and second order systems-time response specifications, steady state error and error constants, response of P, PI, and PID controllers.

UNIT-III

Concept of Stability and Root Locus: The concept of stability, necessary conditions for stability – routh Hurwitz's criterion – limitations of routh's stability – root locus concept – construction of root loci, effect of poles & zeros on stability, case studies.

UNIT-IV

Frequency Domain Analysis: Introduction, correlation between time and frequency response, frequency domain specifications, bode plots, Nyquist stability criterion - gain and phase margin.

UNIT-V

Compensation Techniques: System design and compensation-realization of basic lead, lag and lead-lag cascade compensation in frequency domain.

State Space Analysis of Continuous Systems: Concepts of state, state variables and state model, state models - differential equations & Transfer function models - Block diagrams. Diagonalization, Transfer function from state model, Solving the Time invariant state Equations-State Transition Matrix and its Properties.

Text Books:

- 1. Katsuhiko Ogata, "Modern Control Engineering", 5thedition, Prentice Hall of India Pvt. Ltd., 2010.
- **2.** I. J. Nagrath and M. Gopal, "Control Systems Engineering", 5thedition, New Age International (P) Limited Publishers, 2007.
- 3. "Control Systems" by A. Anand Kumar, Prentice Hall of India Pvt. Ltd.
- 4. Control System Engineering by A. Nagoor Kani, RBA PUB

Reference Books:

- 1. M.Gopal, "Control Systems Principles & Design", 4 th Edition, Mc Graw Hill Education, 2012.
- 2. B. C. Kuo and Farid Golnaraghi, "Automatic Control Systems", 8 th edition, John wiley and sons, 2003.
- 3. Joseph J Distefano III, Allen R Stubberud & Ivan J Williams, "Feedback and Control Systems", 2nd Edition, Schaum's outlines, Mc Graw Hill Education, 2013.
- 4. Graham C. Goodwin, Stefan F. Graebe and Mario E. Salgado, "Control System Design" Pearson, 2000.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

NADAPA - 516 093.

Course Title	CMOS VLSI Design					B. Tech. EC	E VI Sen	n
Course Code	Category	Hours/Week			Credits	Maximum Marks		
2004604	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3	-		3	40	60	100
Mid Exam Dur		End Exam	Duratio	n: 3Hrs				

The main objectives of this course are:

- Basic characteristics of MOS transistor and examines various possibilities for Configuring inverter circuits and aspects of latch-up are considered.
- Design processes are aided by simple concepts such as stick and symbolic diagrams but the key element is a set of design rules, which are explained clearly.
- Circuit parameters which greatly ease the design process. Understand the concepts of scaling MOS circuits.
- Understand FPGA design, synthesis and different case studies.
- Need for Design of Low-Power VLSI Circuits.

	ced for Besign of Bow I ower V Bor enedits.						
Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	Understand the properties, Layout, Stick Diagrams, parameters of MOS devices and						
	Sources of Power Dissipation.						
CO 2	Analyze the inverters, Stick Diagrams, propagation delay, FPGA design flow, Logic						
	synthesis and Power Dissipation.						
CO 3	Apply Design Rules and Layout diagrams, CMOS logic.						
CO 4	Design inverters, layouts, CMOS Logic Structures						
CO 5	Synthesize RTL, logic and high level models.						

UNIT-I

Introduction and Basic Electrical Properties of MOS Circuits: VLSI Design Flow, Introduction to IC technology, Fabrication process: nMOS, pMOS and CMOS. Ids versus Vds Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit. nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, and through one or more pass transistors. Alternative forms of pull-up, The CMOS Inverter, body bias effect, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and Bi-CMOS technology.

UNIT-II

MOS and Bi-CMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout, Generalobservations on the Design rules, 2μ m Double Metal, Double Poly, CMOS/BiCMOS rules, 1.2μ m Double Metal, Double Poly CMOS rules, Layout Diagrams of NAND and NOR gates and CMOS inverter, Symbolic Diagrams- Translation to Mask Form.

UNIT-III

Basic Circuit Concepts: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, some area Capacitance Calculations, The Delay Unit, Inverter Delays, driving large capacitive loads, Propagation

Delays.

Scaling Of MOS Circuits: Scaling models and scaling factors, scaling factors for device parameters, Limitations of scaling.

CMOS Logic Structures: Static CMOS Design (CMOS logic, Pseudo-nMOS logic, Transmission gate logic, Pass transistor logic), Dynamic CMOS Design (Dynamic CMOS logic, Domino CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch Logic)

UNIT-IV

FPGA Design: FPGA design flow, Basic FPGA architecture, FPGA Technologies, Introduction to FPGA Families, Xilinx XC4000 series FPGA, Xilinx Spartan II FPGAs, and Xilinx Vertex FPGA, case studies.

Introduction to synthesis: Logic synthesis, RTL synthesis, High level Synthesis.

UNIT-V

Sources of Power Dissipation: Introduction, Short-Circuit Power Dissipation, Dynamic Power Dissipation, Leakage Power Dissipation, Total power dissipation, Voltage Scaling, Reduction of Switched Capacitance, Reduction of Switching Activity, Need for low-power VLSI Design.

Text Books:

- 1. Kamran Eshraghian, Douglas and A. Pucknell and Sholeh Eshraghian, "Essentials of VLSI Circuits and Systems", Prentice-Hall of India Private Limited, 2005 Edition.
- 2. Sung-Mo Kang, YusufLeblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw- Hill Education, 2003 Edition.

Reference Books:

- 1. Michael D.Ciletti, "Advanced Digital Design with the Verilog HDL", Xilinx DesignSeries, Pearson Education.
- 2. A. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", Kluwer Academic Press, 1995.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 043.

Course	Title	INFORMAT	ION TH	IEORY	B. Tech. EC	E VI Sem			
Course	Code	Category	Но	ours/We	ek	Credits	Maximum Marks		
2004605		PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total
			3	-		3	40	60	100
Mid Ex	am Dur	ation: 90Min					End Exam	Duration	n: 3Hrs
Course	Objecti	ves:							
	• 1	To know variou	s inform	ation me	easures.				
	• 1	o understand v	arious in	nformati	on chan	nels.			
	• 1	o explain diffe	rent sou	rce code	algorith	nms.			
		o familiarize q							
Course		nes: On success					students will be	e able to	
CO 1		stand concepts							on.
		y, Rate of info							,
CO 2	- A	• '		ng Shan	non Enc	oding, Sh	annon Fano. Pi	efix and I	Huffman
	Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms								
CO 3				iscrete	commu	nication cl	nannels using	input, ou	tput and
		Model the continuous and discrete communication channels using input, output and joint probabilities							
CO 4	Analyze quantization and transform coding.								

UNIT-I

Information Theory: Introduction to Information Theory and Coding, Definition of Information Measure and Entropy, Extension of An Information Source and Markov Source, Adjoint of An Information Source, Joint and Conditional Information Measure, Properties of Joint and Conditional Information Measures and A Morkov Source Properties of Joint and Conditional Information measures and a Markov source.

UNIT-II

Source Coding: Source coding theorem, Prefix Codes, Kraft McMillan Inequality property, Encoding of the Source Output, Shannon's Encoding Algorithm, Shannon Fano Encoding Algorithm, Huffman codes, Extended Huffman coding, Arithmetic Coding.

UNIT-III

Information Channels I:Introduction to Information Channels, Equivocation and Mutual Information, Properties of Different Information Channels, Reduction of Information Channels, Properties of Mutual Information and Introduction to Channel Capacity, Calculation of Channel Capacity for Different Information Channels, Shannon's Second Theorem.

UNIT-IV

Information Channels II: Error Free Communication Over Noisy Channel, Error Free Communication Over A Binary Symmetric Channel and Introduction to Continuous Sources and Channels, Differential Entropy and Evaluation of Mutual Information for Continuous Sources

and Channels, Channel Capacity of A Band Limited Continuous Channel.

UNIT-V

Quantization: Introduction to Quantization, Lloyd-Max Quantizer, Companded Quantization, Variable Length Coding and Problem Solving in Quantizer Design, Vector Quantization, Transform Coding-Idea of Transform Coding, Choosing the weights of basis vector, forward transform, Energy preserving, Optimal bit allocation.

Text Books:

- 1. T. M. Cover, J. A, Thomas, "Elements of information theory," Wiely Interscience, 2 nd Edition, 2013
- 2. R. W. Hamming, "Coding and information theory," Prentice Hall Inc., 1986.

Reference Books:

- 1. Bose, "Information Theory, Coding and Cryptography", McGraw hill Education, 2017.
- 2. S. Gravano, "Introduction to Error Control Codes", Oxford, 2007.
- 3. Robert B. Ash, "Information Theory", Dover Publications, 2003.
- 4. Todd k Moon, "Error Correction Coding: Mathematical Methods and Algorithms", Wiley, 2021.

Professor & H.O.D.

Department of E.C.E.

K.S.B.M. College of Engineering

KADAPA - 516 083

Course Title	SENS	SORS A	ND AC	B. Tech. EC	E VI Sem	1		
Course Code	Category	Hours/Week C			Credits	Maximum Marks		
2004606	PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total
		3	-		3	40	60	100
Mid Exam Duration: 90 Min						End Exam	Duratio	n: 3Hrs

- To know the importance of Sensors and Actuators.
- To understand working of magnetic sensors
- · To understand actuators and solenoids
- To explain principles of operation and working of rotary actuators.
- To familiarize controls in NC machine fluidic system

Course	Course Outcomes: On successful completion of this course, the students will be able to							
CO 1	CO 1 Understand the principle of various sensors and actuators.							
CO 2	Compare various sensors and actuators and apply in real time scenario							
CO 3	Model linear actuators and differentiate various solenoids							
CO 4	Analyze the noise in various sensors and actuators, controls in NC machine and fluidic							
	system.							

UNIT-I

Introduction- Classification of Sensors and Actuators - Magnetic Sensors - Linear and Latching Solenoid Actuators - Stepper Motors - Special Magnetic Devices - Rotary and Linear Actuators - Magnetic Materials and Technology - Soft Magnetic Materials - Hard Magnetic Materials - Coating Technologies - Magnetic Materials Market and Applications.

UNIT-II

Magnetic Sensors - Theory of Magnetic Sensors - Magnetic Sensor Analysis - VR Sensors - Solid-State Sensors - Magnetic Sensor Applications - Magnetic Speed Sensor Requirements - Magnetic Speed Sensor Applications - VR Sensor Noise.

UNIT-III

Gas sensors- Optical gas sensor- Metal oxide semiconductor gas sensor- Field effect transistor gas sensor- Piezoelectric gas sensor- Polymer gas sensor- Nano-structured based gas sensors.

UNIT-IV

Rotary Actuators - Disk Rotary Actuators - Disk Rotary Actuator Analysis - Disk Rotary Actuator Design - Disk Rotary Actuator Excitation Electromagnetic Circuit - Disk Rotary Actuator Toothed Magnetic Part - Disk Rotary Actuator PM - Claw Pole Rotary Actuators - Claw Pole Rotary Actuator Analysis - Claw Pole Rotary Actuator Design - Claw Pole Rotary Actuator Excitation Electromagnetic Circuit - Claw Pole Actuator Toothed Magnetic Part - Claw

Pole Actuator PM - Cylindrical Rotary Actuators - Cylindrical Rotary Actuator PM - Cylindrical Rotary Actuator Excitation Electromagnetic Circuit - Cylindrical Rotary Actuator Toothed Magnetic Structure - Rotary Actuator Applications - Disk Rotary Actuator Application - Claw Pole Rotary Actuator Application - Cylindrical Rotary Actuator Application.

UNIT-V

Controls in NC Machines and fluidic control- stepping motors- feedback devices- encoders - resolvers - inductosync -Tachogenerators - principles of fluid logic control -Coanda effect - basic fluidic devices - fluidic logic gates - bistable flipflop - OR and NOR gates - exclusive OR gates - fluidic sensors - backpressure sensor - cone jet proximity sensor - interruptible jet sensor.

Text Books:

- 1. Andrzej M. Pawlak , "Sensors and Actuators in Mechatronics, Design and Applications" , Taylor & Francis Group, 2006
- 2. Andrew Parr, "Hydraulics and Pneumatics", Jaico Publishing House, Mumbai.

Reference Books:

- 1. YoramKoren, 'Computer control of Manufacturing Systems', Tata McGraw Hill Publishers, New Delhi
- 2. Robert H. Bishop, "Mechatronic systems, Sensors and Actuators Fundamentals and Modelling, Taylor & Francis Group, 2007
- 3. Adams, Thomas M., Layton, Richard A., "Introductory MEMS- Fabrication and Applications" -, Spinger, 2010.
- 4. Tai-Ran Hsu, MEMS and Microsystems: Design and manufacture, McGraw-Hill, 2002

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.

Course Title	DIGITAL SIGNAL PROCESSING LAB					B. Tech. ECE VI Sem				
Course Code	Category	Н	ours/We	eek	Credits	Maximum Marks				
2004607	PCC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total		
		-		3	1.5	40	60	100		
		End Exam	Duration	n: 3Hrs						

- To become familiar with MATLAB fundamentals
- To write MATLAB programme for basic DSP operations
- To understand the uses of TMS320C6748 processors
- To write C language code for basic DSP operations and executed using TMS processors

	To write a language code for basic DST operations and executed using TWS processors
Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Analyze discrete/digital signals using mat lab and the basic operations of signal
	processing.
CO 2	Obtain the spectral parameters of windowing functions.
CO 3	Design FIR and IIR filters for desired specifications
CO 4	Design and implement DSP algorithms in software using a computer language such as
	C with TMS320C6748 floating point processor.

List of Experiments: (Minimum of 5 experiments are to be conducted from each part) Software Experiments (PART - A)

- 1. Frequency response of a system described by a difference equation.
- 2. Generation of DTMF Signals.
- 3. To compute power density spectrum of a sequence.
- 4. Convolution of two discrete-time sequences with and without built in command.
- 5. Correlation between two discrete-time sequences with and without built in command.
- 6. DFT of a given signal with and without built in command.
- 7. Design of FIR filter using windowing technique.
- 8. Design of IIR filters using Impulse invariance or bilinear transformation.
- 9. Implementation of a Decimation Process.
- 10. Implementation of a Interpolation Process.

Using DSP Processor kits (Floating point) and Code Composure Studio (CCS) (PART – B)

- 1. Introduction to DSP Processors.
- 2. Generation of Sine wave & Square wave.
- 3. Finding Power and (or) Energy of a given signal.
- 4. Convolution of two discrete-time sequences.
- 5. Correlation between two discrete-time sequences.
- 6. DFT of a given signal
- 7. Design of FIR filter using windowing technique and verify the frequency response of the filter.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 063.

Course Title			VE & O			B. Tech. ECE VI Sem				
Course Code	Category	H	ours/We	eek	Credits	Maximum Marks				
2004608	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total		
		-	-	P	1.5	40	60	100		
Mid Exam Dur	Aid Exam Duration: 90Min					End Exam Duration: 3Hrs				

- To provide knowledge on various types of microwave sources.
- To verify the S-matrix of different Junctions
- To study waveguide and attenuation characteristics.
- To study the characteristics of optical sources and measure optical fiber parameters.

	20 starty the original of optical sources and measure optical most parameters.
Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Analyze the characteristics of different microwave sources.
CO 2	Measure the parameters of wave guide and microwave junctions.
CO 3	Examine the characteristics of optical fiber and sources.
CO 4	Analyze the microwave antenna performance

Part – A (Any 7 Experiments):

- 1. Reflex Klystron Characteristics.
- 2. Gunn Diode Characteristics.
- 3. Attenuation Measurement.
- 4. Directional Coupler Characteristics.
- 5. VSWR Measurement.
- 6. Impedance Measurement.
- 7. Waveguide parameters measurement.
- 8. Scattering parameters of Directional Coupler.
- 9. Scattering parameters of Magic Tee.
- 10. Characteristic of Three Port Circulator

Part – B (Any 5 Experiments):

- 1. Characterization of LED.
- 2. Characterization of Laser Diode.
- 3. Intensity modulation of Laser output through an optical fiber.
- 4. Measurement of Data rate for Digital Optical link.
- 5. Measurement of NA.
- 6. Measurement of losses for Analog Optical link.
- 7. Radiation Pattern Measurement of Horn Antenna.
- 8. Radiation pattern of Microstrip Patch antennas.

Professor & N.O.D.

Department of E.C.E.

R.S.R.M. College of Engineering

KADAPA - 516 063

Course Title	VL	VLSI Design Laboratory					B. Tech. ECE VI SEM				
Course Code	Category	H	ours/We	eek	Credits	Maxin	num Marks				
2004609	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total			
			-	3	1.5	40	60	100			
		End Exam	Duration	n: 3Hrs							

The main objectives of this course are:

- Understanding basic laws and rules of designing the digital circuits.
- Analyzing the Concepts of Simulation Results, RTL Schematic

Course	Course Outcomes: On successful completion of this course, the students will be able to							
CO 1	Design and simulate basic CMOS circuits like inverter and basic logic gates.							
CO 2	Design and simulate adders and subtractors.							
CO 3	Realize various flip-flops and encoder & decoder.							
CO 4	Generate RTL schematic for the combinational & sequential Circuits.							
CO 5	Verify the logic using FPGA.							

NOTE:

- The students are required to design and implement **any 12 Experiments** using Xylinx Vivado tool/Industry Equivalent Standard Software.
- The students are required to implement and verify its synthesis of any FOUR Experiments using FPGA.
- List of Experiments:
- 1. Design and Implementation of a CMOS Inverter.
- 2. Design and Implementation of an Universal Gates
- 3. Design and Implementation of an XOR and XNOR Gates.
- 4. Design and Implementation of a Boolean expression $Y = \overline{(AB + CD + E)}$
- 5. Design and Implementation of Half-adder and Half-subtractor.
- 6. Design and Implementation of 1-bit Full Adder.
- 7. Design and Implementation of 4-bit Ripple Carry Adder.
- 8. Design and Implementation of 2-bit Binary multiplier.
- 9. Design and Implementation of 2*1 MUX.
- 10. Design and Implementation of 2 to 4 Decoder
- 11. Design and Implementation of RS-Latch
- 12. Design and Implementation of D-Flip-flop
- 13. Design and Implementation asynchronous counter
- 14. Design and Implementation of static RAM cell
- 15. Design and Implementation of Differential Amplifier.

Lab Requirements:

- 1. Software: Xylinx Vivado tool/Industry Equivalent Standard Software.
- **2. Hardware:** Personal Computer with necessary peripherals, configuration and operating System and FPGAs.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093

Course Title	Constitution of India (Mandatory Course)					B. Tech. ECE VI Sem				
Course Code	Category	Hours/Week Credits				Maxin	mum Marks			
20MC509	MC	MC L T		P	С	Continuous Internal Assessment	End Exams	Total		
		2	0	0	0	40	00	40		
						End Exam	Duration	n: -		

Course Objectives: The main objective of the course to learn

- To realize the significance of the constitution of India to students from all walks of life and help them to understand the basic concepts of Indian constitution.
- To identify the importance of fundamental rights as well as fundamental duties.
- To understand the functioning of Union, State and Local Governments in the Indian federal system.
- To learn procedure and effects of emergency, composition and activities of election commission and amendment procedure.

Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Describe the historical background of the constitution making and its importance for
	building a democratic India.
CO 2	Explain the functioning of three wings of the government i.e., executive, legislative and
	judiciary.
CO3	Explain the value of the fundamental rights and duties for becoming good citizen of
	India.
CO 4	Analyze the decentralization of power between central, state and local self government.
CO5	Apply the knowledge in strengthening of the constitutional institutions like CAG,
	Election Commission and UPSC for sustaining democracy

Unit - 1:

Introduction to Indian Constitution: Constitution meaning of the term, Indian Constitution – Sources and constitutional history, Features –

Citizenship, Fundamental Rights and Duties, Directive Principles of State Policy.

Unit - 2:

Union Government and its Administration Structure of the Indian Union: Center-State

relationship, President: Role, power and position, PM and Council of ministers, Cabinet a nd Central Secretariat, LokSabha, RajyaSabha, The Supreme Court and High Court: Powers and Functions.

Unit - 3:

State Government and its Administration Governor – Role and Position – CM and Council of ministers, State Secretariat: Organization, Structure and Functions. Unit - 4:

Local Administration: District's Administration Head – Role and Importance, Municipalities – Mayor and role of Elected Representative – ZillaPanchayat, Elected officials and their roles, CEO ZilaPanchayat: Block level Organizational Hierarchy – (Different departments), Village level – Role of Elected and Appointed officials.

Unit - 5:

Election Commission: Election Commission- Role of Chief Election Commissioner and Election Commissioner State Election Commission:, Functions of Commissions for the welfare of SC/ST/OBC and women.

Textbooks

- 1. M.V.Pylee, "Introduction to the Constitution of India",4th Edition, Vikas publication,2005.
- 2. Durga Das Basu(DD Basu), "Introduction to the constitution of India", (Student Edition), 19th edition, Prentice-Hall EEE, 2008.

Reference Books:

- Durga Das Basu, Introduction to the Constitution of India, Prentice Hall of India Pvt.
 Ltd.. New Delhi
- Subhash Kashyap, Indian Constitution, National Book Trust
- J.A. Siwach, Dynamics of Indian Government & Politics
- D.C. Gupta, Indian Government and Politics
- H.M.Seervai, Constitutional Law of India, 4th edition in 3 volumes (Universal Law Publication)
- J.C. Johari, Indian Government and Politics Hans
- J. Raj IndianGovernment and Politics
- M.V. Pylee, Indian Constitution Durga Das Basu, Human Rights in Constitutional Law, Prentice Hall of India Pvt. Ltd.. New Delhi
- Noorani, A.G., (South Asia Human Rights Documentation Centre), Challenges to Civil Right), Challenges to Civil Rights Guarantees in India, Oxford University Press 2012.

E-Resources:

- nptel.ac.in/courses/109104074/8
- nptel.ac.in/courses/109104045/
- nptel.ac.in/courses/101104065/
- www.hss.iitb.ac.in/en/lecture-details
- www.iitb.ac.in/en/event/2nd-lecture-institute-lecture-series-indian-constitution

Professor & H.O.D.

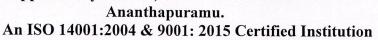
Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.



K.S.R.M. COLLEGE OF ENGINEERING (UGC-AUTONOMOUS) Kadapa, Andhra Pradesh, India—516 003 Approved by AICTE, New Delhi & Affiliated to JNTUA,





Department of ECE M.Tech Embedded Systems and VLSI Course Structure

		Semester-I							
S.No	Course Code	Course Name	Category	L	Т	P	IM	EM	Credits
1.	2284101	RTL Simulation and Synthesis With PLDs	PCC	3	0	0	40	60	3
2.	2284102	Microcontrollers and Programmable Digital Signal Processors	PCC	3	0	0	40	60	3
3.	2284103	Research methodology and IPR	-	2	0	0	40	60	2
	Profe	essional Elective Course-I							
4.	2284104	Parallel Processing							
	2284105	Digital Signal and Image Processing					40	60	2
	2284106	VLSI Signal Processing	PEC	3	0	0	40	60	3
	2284107	Design for testability							
	Profe	ssional Elective Course-II							
5.	2284108	Programming Languages for Embedded Systems							
	2284109	Micro-Electro Mechanical systems.	PEC	3	0	0	40	60	3
	2284110	CAD of Digital System							
	2284111	CPLD, FPGA Architectures and Applications.							
6.	2284112	RTL Simulation and Synthesis with PLDs Lab	PCC	0	0	4	50	50	2
7.	2284113	Microcontrollers and Programmable Digital Signal Processors Lab	PCC	0	0	4	50	50	2
8.	2270A02	Disaster Management	AC				40		0
									18

		Semester-II							
S.No.	Course Code	Course Name	Category	L	Т	P	IM	EM	Credit
1.	2284201	Analog and Digital CMOS VLSI Design	PCC	3	0	0	40	60	3
2.	2284202	Embedded and Real Time Operating Systems	PCC	3	0	0	40	60	3
	Profe	essional Elective Course-III							
	2284203	Memory Architectures							
3.	2284204 2284205	Advanced Computer Architecture SoC Design	PEC	3	0	0	40	60	3
	2284206	Low Power VLSI Design							
	Profess	ional Elective Course-IV							
4.	2284207 2284208	Communication Buses and Interfaces Network Security and Cryptography	PEC	3	0	0	40	60	3
	2284209	Physical design automation							
	2284210	Nano Electronics							
5.	2284211	Analog and Digital CMOS VLSI Design Lab	PCC	0	0	4	50	50	2
6.	2284212	Real Time Operating Systems Lab	PCC	0	0	4	50	50	2
7.	2284213	Technical Seminar	PCC	0	0	4	100	0	2
8.	2270A01	English for Research Paper Writing	AC				40		0
									18

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. Coilege of Engineering

KADAPA - 516 083

		Semest	er-III						
S.No.	Course Code	Course Name	Category	L	T	P	IM	EM	Credits
		Professional Elective Course-V							
	2284301	IOT and its Applications						60	
	2284302	Hardware Software co-design			0	0	40		
1.	2284303	Artificial Intelligence	PEC	3					3
	2284304	RFIC Design							
		Open Elective Course							
	2271305	Business Analytics							
	2271306	Industrial Safety				0	40	60	
	2271307	Operations Research		3	0				
2.	2271308	Cost Management of Engineering Projects	OEC						3
	2271309	Composite Materials							
	2271310	Waste to Energy							
3.	2284311	Dissertation Phase-I	PR	0	0	20	100	0	10
4	2254312	Co-Curricular activities							2
									18

		Semester-IV							
S.No.	Course Code	Course Name	Category	L	Т	P	IM	EM	Credits
1.	2284401	Dissertation Phase II	PR	0	0	32	50	50	16
									16



Course Title	RTL SIMUI WITH PLD		N AND	M. Tech. ES &VLSI I Sem				
Course Code	Category	Ho	urs/We	ek	Credits	Maximum Marks		
2284101	PCC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Dur		End Exam	Duration	3Hrs				

- To introduce Verilog HDL for the design and functionality verification of a digital circuit.
- > To understand the design of data path and control circuits for sequential machines
- > To introduce the concept of realizing a digital circuit using PLDs

Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Understand the Static Timing Analysis and clock issues in digital circuits
CO 2	Appreciate the analysis of finite state machine of a controlling circuit
CO 3	Develop the Verilog HDL to design a digital circuit.
CO 4	Verify the functionality of the digital designs using PLDs.

UNIT I

Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDL Gate level modeling: Built in primitive gates, switches, gate delays Data flow modeling: Continuous and implicit continuous assignment, delays Behavioral modeling: Procedural constructs, Control and repetition Statements, delays, function and tasks.

UNIT II

Digital Design: Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider. FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT III

ASIC Design Flow: Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

UNIT IV

Static Timing Analysis: Timing paths, Meta-stability, Clock issues, Need and design strategies for multi-clockdomain designs, setup and hold time Violations, steps to remove Setup and hold time violations.

UNIT V

Digital Design using PLD"s: ROM, PLA, PAL- Registered PAL"s, Configurable PAL"s, GAL. CPLDs: Features, Programming and Applications using Complex Programmable logic devices. FPGAs: Field Programmable gate arrays Logic blocks, routing architecture, design flow.

TEXTBOOKS:

- 1. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis", 2nd Edition, 2003.
- 2. Charles H.Roth, "Fundamentals of Logic Design", Cengage Learning, 5th Edition, 2010.
- 3. Bhasker J, "Verilog HDL Synthesis A Practical Primer", 1st edition, 1998.

REFERENCES:

- 1. Donald D Givone, "Digital Principles and Design", TMH, 2016
- 2. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books,2002.
- 3. Richard S. Sandige, "Modern Digital Design", MGH, International Edition, 1990

Professor & H.O.D.

Department of E.C.E.

K.S.B.M. College of Engineering

KADAPA - 616 093

Course Title	MICROCO PROGRAM PROCESSO	MABL			SIGNAL	M. Tech. ES &VLSI I Sem			
Course Code	Category	Ho	urs/We	ek	Credits	Maxin	Maximum Marks		
2284102	PCC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total	
		3			3	40	60	100	
Mid Exam Dur	ation: 2Hrs					End Exam	Duration	3Hrs	
Course Objecti	ves:								

- > To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- > To be able to identify and characterize architecture of Programmable DSP Processors.
- > To develop small applications by utilizing the ARM processor core and DSP processor based platform.

Course	Course Outcomes: On successful completion of this course, the students will be able to								
CO 1	Compare and select ARM processor core based SoC with several features/peripherals								
	based on requirements of embedded applications.								
CO 2	Identify and characterize architecture of Programmable DSP Processors								
CO3	Develop small applications by utilizing the ARM processor core and DSP processor								
	based platform.								

UNIT I

ARM Cortex-M3 processor: Applications, Programming model - Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT III

LPC 17xx Microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing.

TEXT BOOKS:

- 1. Joseph Yiu, "The definitive guide to ARM Cortex M3", Elsevier, 2nd Edition.
- 2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition
- 3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication

REFERENCE BOOKS:

- 1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
- 2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
- 3. Technical References and user manuals on www.arm.com.

Professor & M.O.D.

Department of E.C.E.

B.B.M. College of Engineering

KADAPA - 616 003

Course Title	RESEARCH AND IPR	METH	ODOL	M. Tech ES	& VLSI	I Sem		
Course Code	Category	H	ours/W	eek	Credits	Maxi	mum Ma	rks
2284103	PCC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total
		2	0		2	40	60	100
Mid Exam Dui		End Exa	am Durat	ion: 3Hrs				

- > To understandresearchproblemformulation.
- > To Analyzeresearch related information
- > To Followresearchethics
- To understanding that when IPR would take such important place in growth of individuals &nation, it is needless to emphasis the need of information about Intellectual Property Right to bepromoted amongstudents in general & engineering in particular.
- To understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Understand research problem formulation.
CO 2	Analyze research related information
CO 3	Followresearchethics
CO 4	Apply PatentRights in filing.
CO 5	Describe new developments in IPR.

UNITI

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting are search problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, Analysis, interpretation, Necessary instrumentations.

UNIT II

Effective literature studies approaches, Analysis Plagiarism and Research ethics. Effective technical writing, How to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright, Process of Patenting and Development: Technological research, Innovation, Patenting, Development. International Scenario: International Cooperation on Intellectual Property, Procedure for grants of patents, Patent in gender PCT.

UNITIV

Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent in formation and databases, Geographical Indications.

UNIT V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

- 1. Stuart Melville and Wayne Goddard, "Research Methodology: An Introduction for Science & Engineering students"
- 2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- 3. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners", 2nd Edition,

REFERENCE BOOKS:

- 1. Mayall, "Industrial Design", Mc Graw Hill, 1992.
- 2. Niebel, "Product Design", Mc Graw Hill, 1974.
- 3. Asimov, "IntroductiontoDesign", PrenticeHall, 1962.
- 4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
- 5. T. Ramappa, "Intellectual Property Rights Under WTO", S.Chand, 2008

Professor & M.O.D.

Department of E.C.E.

N.S.R.M. College of Engineering

KADAPA - 516 093

Course Title	PARALLEI	PROC	CESSIN	M. Tech ES & VLSI I Sem				
Course Code	Category	Но	urs/We	ek	Credits	Maximum Marks		
2284104	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Dur		End Exam	Duration	: 3Hrs				

- > Tooverview of the architectures and communication networks employed in parallel computers.
- The course covers the foundations for development of efficient parallel algorithms, including examples from relatively simple numerical problems, sorting, and graph problems.

Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Understand parallel processing and pipelining techniques.
CO 2	Identify limitations of different architectures of computer
CO 3	Analysis quantitatively the performance parameters for different architectures
CO 4	Investigate issues related to compilers and instruction set based on type of architectures
CO 5	Develop parallel programming techniques.

UNIT I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

UNIT II

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT III

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT IV

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

UNIT V

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXT BOOKS:

- 1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
- 2. Kai Hwang, "Advanced Computer Architecture", TMH
- 3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.

REFERENCE BOOKS:

- 1. William Stallings, "Computer Organization and Architecture, Designing for performance "Prentice Hall, Sixth edition
- 2. Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
- 3. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan

Professor & M.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003

Course	Title	DIGITAI		IAL AN ESSIN	M. Tech. ES & VLSI I Sem				
Course	Code	Category	Hours/Week			Credits	Maximum Marks		
22841	105	PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total
			3	0		3	40	60	100
Mid Exa	ım Dur	ation: 2Hrs					End Exam	Duration	n: 3Hrs
Course	 To study the discrete time signals and system in various domains To learn the concepts of design of digital filtering To study different image enhancement, Restoration and compression techniques To understand image segmentation algorithms Course Outcomes: On successful completion of this course, the students will be able to								
CO 1		ze discrete-time							Fourier)
CO 2									(durier)
CO 3	Design the digital filters (both IIR and FIR) from the given specifications Analyze the quantization effects in digital filters and understand the basics of image sampling, quantization and image transforms.								
CO 4		stand the conce olor Image proc		nage enh	anceme	nt, image	restoration, image	age segme	entation
CO 5	Analyz	ze various imag	e compr	ession to	echnique	es			

UNIT I

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, Fast Fourier Transform using Decimation in Time (DIT) and Decimation in Frequency (DIF) Algorithms.

UNIT II

IIR Digital Filters: Introduction, Analog filter approximations—Butterworth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.

FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

UNIT III

Analysis Of Finite Word length Effects: The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating- Point Numbers ,Analysis of Coefficient Quantization effects.

Introduction To Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, Image Transforms: 2D-DFT, DCT, Haar Transform.

UNIT IV

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using

frequency domain filters, Selective filtering.

Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.

Image Segmentation: Fundamentals, point, line, edge detection, thresholding, and region based segmentation.

UNIT V

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding. Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

TEXT BOOKS:

- 1. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Principles, Algorithms, and Applications, Pearson Education, PHI, 2007.
- 2. S. K. Mitra. "Digital Signal Processing A Computer based Approach", TMH, 3rd Edition, 2006
- 3. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson Education, 2011.

REFERENCE BOOKS:

- 1. Andreas Antoniou, "Digital Signal Processing", TATA Mc Graw Hill, 2006
- 2. M H Hayes, "Digital Signal Processing", Schaum"s Outlines, TATA Mc Graw Hill, 2007.
- 3. Anil K. Jain, "Fundamentals of Digital Image Processing,", Prentice Hall of India, 2012.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 616 003.

Course	Title	VLSI SIGN.	AL PRO	OCESSI		M. Tech ES & VLSI I Sem			
Course	Code	Category	Ho	urs/We	ek	Credits	Maxim	ium Mar	ks
2284106		PEC	L	T	P	C	Continuous Internal Assessment	Total	
			3			3	40	60	100
Mid Exa	Mid Exam Duration: 2Hrs End Exam Duration: 3Hrs								
Course	Objecti	ves:							
	> To u	understand the s	static, sr	nall sign	al and	large signa	l modeling of N	AOS Tran	sistor.
		understand the I				0 0	C		
		understand the				pects of pro-	cessors.		
Course	Outcon	ies: On success	ful com	pletion	of this	course, the	students will be	e able to	
CO 1	Ability to modify the existing or new DSP architectures suitable for VLSI.								
CO 2	Under	stand the conce	pts of fo	lding ar	nd unfo	lding algori	thms and appli	cations.	
CO 3		ze to implement			August 1975 and the second				

Develop Low power design aspects of processors for signal processing and wireless

UNIT I

CO 4

applications.

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel ProcessingIntroduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT II

Folding and Unfolding: Folding - Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems.

Unfolding - Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV

Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution algorithm by Inspection

UNIT V

Digital lattice filter structures, Bit level arithmetic, Architecture, Redundant arithmetic. Numerical Strength reduction, Synchronous wave and asynchronous pipe lines, Low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

TEXT BOOKS:

- 1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", Wiley, Inter Science, 1999.
- 2. Mohammad Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.

REFERENCE BOOKS:

- 1. S. Y. Kung, H. J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
- 2. Jose E. France, Yannis Tsividls, "Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing", Prentice Hall, 1994.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.

Course	Title	DESI	GN FOI	R TEST	ABIL	ITY	M. Tech. ES	&VLSI	
Course	Code	Category	Но	urs/We	ek	Credits	Maxin	num Mar	ks
2284	107	PEC	L	Т	P	C Internal Er		End Exams	Total
			3			3	40	60	100
Mid Exa	am Dur	ation: 2Hrs					End Exam	Duration	3Hrs
Course	Objecti	ves:							
	> To	panalyze the di	gital circ	cuits wit	h the p	resence of	faults.		
	> To	generate the t	est patte	rns.					
		understand the			trollah	ility and oh	servahility		
						inty and ob	servaumity.		
~		determine the							
							students will be		
CO 1	Design simula		includi	ng vario	us leve	els of mode	ling and differe	ent approa	ches for
CO 2	Analyz	e the digital cir	cuits wi	ith the p	resence	e of faults a	nd evaluation o	of given te	st set
		lt coverage.		r				or green te	Bt BCt
CO 3			r detecti	ng singl	e stuck	faults in c	ombinational a	nd seguen	tiol
	circuits		r detecti	ing singi	e staci	c raures in c	omomational a	na sequen	ıtıaı
CO 4	Descri	be controllabili	ty and o	bservab	ility an	d schemes	for introducing	testability	y into
							vith ease and in		
	covera						•	-F-0 . • Ide	
CO 5	Determ	nine built in sel	f test (B	IST) and	d differ	ent approac	ches for introdu	icing BIS	Γ into

UNIT I

Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

logic circuits memories and embedded cores.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT-V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

TEXT BOOKS:

- 1. Miron A bramovici, Melvin A. Breur, Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
- 2. Alfred Crouch., "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall.

REFERENCE BOOKS:

- 1. Robert J. Feugate, Jr., Steven M. Mentyn, "Introduction to VLSI Testing", Prentice Hall, Englehood Cliffs, 1998.
- 2. Fault Tolerant & Fault Testable Hardware Design- Parag K. Lala, PHI, 1984

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering KADAPA - 516 003.

Course Title	PROGRAMN EMBEDDED			M. Tech. ES &VLSI I Sem				
Course Code	Category	Ho	urs/We	ek	Credits	Maxin	num Mar	ks
2284108	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Dui	ration: 2Hrs		End Exam	Duration	: 3Hrs			

- > To explore the difference between general purpose programming languages and Embedded Programming Language.
- > To provide case studies for programming in embedded systems.

Course Outcomes: On successful completion of this course, the students will be able to							
CO 1	CO 1 Understand the basics of Embedded C with reference to 8051.						
CO 2	Understand how to handle control and data pins at hardware level.						
CO3	Capable of introducing into objective nature of Embedded C.						
CO 4	Understand the specifications of real time embedded programming with case studies						

UNIT I

Programming Embedded Systems in C Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What"s in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT II

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT III

Adding Structure to your Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the "Hello Embedded World" example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT IV

Meeting Real-Time Constraints Introduction, Creating "hardware delays" using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for "timeout" mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT V

Case Study: Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

- 1. Michael J. Pont "Embedded C", A Pearson Education
- 2. Mazidi, "PIC Microcontroller and Embedded Systems: Using assembly and C for PIC 18.

REFERENCE BOOKS:

- 1. Mazidi, "The 8051 Microcontroller and Embedded Systems: Using Assembly and C".
- 2. Michael Barr, "Programming Embedded Systems in C & C++".

Professor & H.O.D.

Department of E.C.E.

K.S.B.M. College of Engineering

KADAPA - 516 083.

Course Title	MICRO-E		RO MI TEMS	ECHA	M. Te	ch ES &	VLSI I Sem		
Course Code	Category	Н	ours/We	eek	Credits	Maximum Marks			
2284109	PEC	·L	T	P	C	Continuous Internal Assessment	End Exams	Total	
		3	0		3	40	60	100	
Mid Exam Duration: 2Hrs						Enc	d Exam I	Ouration: 3Hrs	

- > Able to know a new and upcoming interdisciplinary area.
- > To understand generating better electronic gadgets
- Able to know technologies involving miniaturized Electrical, Mechanical and Electro-mechanical devices
- To understand a new stream of Electronics-MEMTRONICS.

Course	Outcomes On successful and Id. California						
Course	urse Outcomes: On successful completion of this course, the students will be able to						
CO 1	A new and upcoming interdisciplinary area.						
CO 2	Generating better electronic gadgets						
CO 3	Technologies involving miniaturized Electrical, Mechanical and Electro-mechanical devices						
CO 4	A new stream of Electronics-MEMTRONICS						

UNIT I

Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of MEMS to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatibility of MEMS with VLSI Applications in Electronics, Broad Advantages and Disadvantages of MEMS from the point of Power Dissipation, Leakage etc.

UNIT II

Review of Mechanical Concepts like Stress, Strain, Bending Moment, and Deflection Curve. Differential equations describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with voltage in C.L, Deflection Vs Voltage Curve, Critical Deflection, Description of the above w.r.t. Fixed Beams. Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT III

Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT IV

MEM Circuits & Structures for Simple GATES – AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters.

Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT V

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

TEXT BOOKS:

- 1. Gabriel. M. Reviez, R.F. "MEMS Theory", Design and Technology", Jhon Wiley & Sons, 2003.
- 2. Thimo Shenko, "Strength of Materials", CBS Publishers & Distributors.
- 3. K. Pitt, M.R. Haskard, "Thick Film Technology and Applications", 1997.

REFERENCE BOOKS:

- 1. Wise K.D. (Guest Editor), "Special Issue of Proceedings of IEEE", Vol.86, No.8, Aug 1998.
- 2. Ristic L. (Ed.) Sensor Technology and Devices, Artech House, London 1994

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 083

Course Title	CAD O	F DIGI	TAL S	M. Tech ES & VLSI I Sem					
Course Code	Category	Н	ours/W	eek	Credits	Ma	Maximum Marks		
2284110	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total	
		3	0		3	40	60	100	
Mid Exam Duration: 2Hrs						Enc	d Exam I	Ouration: 3Hrs	

- ➤ To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI Systems.
- > To study various phases of CAD, including simulation, physical design, test and Verification.
- > To be able to demonstrate the knowledge of computational algorithms and tools for CAD.

Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	Fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.						
CO 2	Understand various phases of CAD, including simulation, physical design, test andverification.						
CO 3	Demonstrate knowledge of computational algorithms and tools for CAD.						

UNITI

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods, Status of Fabrication Process, Issues related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development.

UNIT II

VLSI design automation tools – Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph theory and Computational complexity, Tractable and intractable problems.

UNIT III

General purpose methods for combinational optimization — Partitioning—Problem Formulation ,Classification of Partitioning Algorithms, Group Migration Algorithms , Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning Floor planning—Chip planning, Pin Assignment , Integrated Approach, Placement—Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms , Partitioning Based Placement Algorithms, Performance Driven Placement, Routing—Global Routing,Problem Formulation,Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.

UNIT IV

Simulation- Gate- level Modelling and Simulation, Switch-level Modeling and Simulation, Logic Synthesis and Verification - Introduction to Combinational Logic Synthesis , Binary-decision Diagrams, Two-level Logic Synthesis, High-level Synthesis- Hardware Models for High level

Synthesis , Internal Representation of the Input Algorithm , Allocation, Assignment and Scheduling.

UNIT V

MCMs-VHDL-Verilog-implementation of adders, Subtractors, Multiplexers, Demultiplexers and counters using VHDL.

TEXT BOOKS:

- 1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".
- 2. S.H. Gerez, "Algorithms for VLSI Design Automation".

REFERENCE BOOKS:

- 1. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis"
- 2. Navabi, "VHDL Analysis & Modeling of digital systems"

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 616 083.

Course Title	CPLD, FPC	GA ARG			RS AND	M. Tech. ES	1. Tech. ES & VLSI I Sem		
Course Code	Category	Но	ours/We	eek	Credits	Maximum Marks			
2284111	PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total	
		3	0		3	40	60	100	
Mid Exam Dur			En	d Evam I	Juration: 3Hrs				

- > Implement given task using FPGA
- Develop test pattern to test the FPGA
- > Design a product level approach utilizing FPGAs.

Course	urse Outcomes: On successful completion of this course, the students will be able to							
CO 1	Differentiate between ROM,PAL,PLA,SPLD,CPLD,FPGA							
CO 2	Compare the features of Various CPLDs interms of their architecture, Logic blocks							
CO 3	Compare the features of Various FPGAs interms of their Architecture, Configurable logic block and routing.							
CO4	Gain knowledge on routing algorithms adopted in FPGAs.							
CO5	Test a particular PLD using various techniques like design validation, Timing verification.							

UNIT I

Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNITIII

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logicblocks and features of Altera flex logic 10000 series CPLD's, max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypres flash 370 device technology, lattice PLSI's architectures.

UNIT IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulatedannealing.Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps .Verification: introduction, logic simulation, design validation, timing verification .Testing

concepts: failures, mechanisms and faults, fault coverage, ATPG methods, and programmability failures.

TEXTBOOKS:

- 1. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
- 2. S. Trimberger, Edr, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.

References:

- 1. Old Field, R. Dorf, "Field Programmable Gate Arrays", John Wiley & Sons, New york, 1995.
- 2. Brown, R. Francis, J. Rose, Z. Vransic, "Field Programmable Gate array", Kluwer Publn, 1992.
- 3. Manuals from Xilinx, Altera, AMD, Actel.

Professor & M.O.D.

Department of E.C.E.

M.S.R.M. College of Engineering

KADAPA - 516 093.

Course Title	RTL SIMUI WITH PLD		N AND	M. Tech. ES &VLSI I Sem				
Course Code	Category	Ho	urs/We	ek	Credits	Maximum Marks		
2284112	PCC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
				4	2	50	50	100
						End Exam	Duration	: 3Hrs

- > To implement the Verilog code for combinational and sequential circuits.
- > To implement the Verilog code for Discrete Fourier Transform/FFT algorithm
- > To design FSM, Vending Machine.

Course	Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	To design various combinational and sequential circuits.						
CO 2	To design FSM machines, Vending machines.						
CO 3	Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.						
CO 4	Realize single port SRAM in Verilog						
CO 5	Implement UART/USART in Verilog.						

LISTOFEXPERIMENTS:

- 1. Verilog implementation of 8:1 Mux/Demux,
 - 2. Verilog implementation of Full Adder, 8-bit Magnitude comparator.
 - 3. Verilog implementation of 3-bit Synchronous Counters.
 - 4. Verilog implementation of Parity generator.
 - 5. Sequence generator/detectors, Synchronous FSM Mealy and Moore machines.
 - 6. Vending machines Traffic Light controller, ATM, elevator control.
 - 7.PCI Bus & arbiter and downloading on FPGA.
 - 8.UART/ USART implementation in Verilog.
 - 9. Realization of single port SRAM in Verilog.
 - 10. Verilog implementation of Arithmetic circuits like serial adder/ subtractor.
 - 11. Verilog implementation of paralleladder/subtractor, serial/parallel multiplier.
 - 12. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Professor & N.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 063.

Course Title		MICROCO PROGRAM PROCESSO	MABL	E DIGI	M. Tech. ES & VLSI I Sem				
Course	Code	Category	Hours/Week			Credits	Maxin	ks	
2284113		PCC	L T P		C	Continuous Internal Exams To		Total	
			-		4	2	50	50	100
	End Exam Duration: 3Hrs								
 Course Objectives: To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications. To be able to identify and characterize architecture of Programmable DSP Processors To develop small applications by utilizing the ARM processor core and DSP processor based platform. 									
Course CO 1		nes: On success							
COT		Install, configure and utilize tool sets for developing applications based on ARM processor Core SoC and DSP processor.							
CO 2		op prototype cortex M3 and DS					and off chip pe	eripherals	on

LIST OF ASSIGNMENTS:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain

- 1. Blink an LED with software delay, delay generated using the Sys Tick timer.
- 2. System clock real time alteration using the PLL modules.
- 3. Control intensity of an LED using PWM implemented in software and hardware.
- 4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
- 5. UART Echo Test.
- 6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
- 7. Temperature indication on an RGB LED.
- 8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
- 9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
- 10. System reset using watchdog timer in case something goes wrong.
- 11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6748 evaluation kits and using Code Composer Studio (CCS)

- 1. To develop an assembly code and C code to compute Euclidian distance between any two points
- 2. To develop assembly code and study the impact of parallel, serial and mixed execution
- 3. To develop assembly and C code for implementation of convolution operation
- 4. To design and implement filters in C to enhance the features of given input sequence (signal C. F.

G. W. S.R.M. College of Engineer MADAPA - 516 00

Course Title	ANALO CMOS		DIGIT DESIGI		M. Tech. ES	& VLSI I	I Sem	
Course Code	Category	Ho	urs/We	ek	Credits	Maxim	um Marl	KS
2284201	PCC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Duration: 2Hrs						End Exam D	uration:	3Hrs

- ➤ To teach fundamentals of CMOS Digital integrated circuit design such as importance of Combinational MOS logic circuits, and Sequential MOS logic circuits.
- ➤ To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.
- ➤ Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

Course	Course Outcomes: On successful completion of this course, the students will be able to					
CO 1	Appreciate the trade-offs involved in analog integrated circuit design.					
CO 2	Understand and appreciate the importance of noise and distortion in analog circuits.					
CO 3	Analyze complex engineering problems critically in the domain of analog IC design for conducting research.					
CO 4	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,					
	Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.					
CO 5	Solve engineering problems for feasible and optimal solutions in the core area of digital					
	ICs.					

Digital CMOS Design:

UNIT I

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption.

UNIT II

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT III

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR

flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design

UNIT IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gatestage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT V

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP.

TEXT BOOKS:

- 1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
- 2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
- 3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

REFERENCE BOOKS:

- 1. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
- 2. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
- 3. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rd Edition.
- 4. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 616 063.

Course Title	EMBEDDED AND REAL TIME OPERATING SYSTEMS					M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week Credits			Maximum Marks			
2284202	PCC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3	-		3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

- > The main objective of the course is to get students familiar with the typical problems and constraints that arise when designing and developing embedded systems
- The course will also introduce theoretical and practical solutions to these typical problems that the students are expected to master and be able to apply to realistic case studies.

Course Outcomes: On successful completion of this course, the students will be able to						
CO 1	Understand the fundamental concepts of a embedded system, General Purpose					
	Processors and Embedded RTOS Concepts.					
CO 2	Apply embedded system concepts in industry, medicine, and defence.					
CO 3	Analyze the embedded design models and Design Technology.					
CO 4	Design custom single purpose processors.					

UNIT I

Introduction: Embedded systems overview, Design challenge, Processor technology, IC technology, Design technology. RT-Level combinational logic, Sequential logic (RT-Level), Custom single purpose processor design (RT-Level), optimizing custom single purpose processors.

UNIT II

General Purpose Processors: Basic architecture, Operation, Programmer"s View, Development environment, Application specific Instruction Set processors (ASIPs).

UNIT III

State Machine and Concurrent Process models: Introduction, Models Vs Languages, Finite State Machine with Data path model (FSMD), Using State Machines, Program State Machine (PSM), Concurrent Process Model, Concurrent Processes, Communication among processors, Synchronization among processes, Implementation, Data flow model, Real-time Systems.

UNIT IV

Design Technology: Introduction, Automation-The parallel evolution of complication and synthesis, Logic, RT, Behavioral synthesis, System synthesis and hardware/software codesign, Verification of hardware/software co-simulation, Reuse of intellectual property cores.

UNIT V

Embedded RTOS Concepts: Architecture of the Kernel, Tasks and Task Scheduler, interrupt service routines, Semaphores, Mutex, Mail boxes, Message Queues, Event Registers, Pipes, Signals.

TEXT BOOKS:

- 1. Frank Vahid, Tony D. Givargis, "Embedded Systems Design A Unified Hardware/Software Introduction", John Wiley & Sons. Inc. 2002.
- 2. Dr. K.V.K.K. Prasad, "Embedded / Real-Time Systems: Concepts, Design and Programming", Dreamtech Publications.

REFERENCE BOOKS:

- 1. Raj Kamal, "Introduction to Embedded Systems", TMH, 2002.
- 2. David E. Simon, "An Embedded Software Primer", 1st Edition, Addison Wesley Professional, 2007.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 083

Course Title	MEMO	ORY AI	RCHIT	RES	M. Tech. ES & VLSI II Sem					
Course Code	Category	Hours/Week			Credits	Maximum Marks				
2284203	PEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total		
		3			3	40	60	100		
Mid Exam Du	ration: 2Hrs				End Exam Duration: 3Hrs					
Course Object	ives:									
To understand the architectureanddesignsemiconductor memorycircuitsandsubsystems										

Course	Course Outcomes: On successful completion of this course, the students will be able to										
CO 1	Select architecture and design semiconductor memory circuits and subsystems.										
	Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.										
CO 3	Analyze the state-of-the-art memory chip design										

RandomAccessMemoryTechnologies:

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOSSRAM Architecture, MOSSRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT II

DRAMs, MOS DRAM Cell, Bi CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory Controllers

UNIT III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT IV

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing

UNIT V

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D&3D), Memory Stacks, Memory Testing and Reliability Issues.

TEXTBOOKS:

- 1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
- 2. Kiyoo Itoh, "VLSI Memory Chip Design", Springer International Edition

REFERENCEBOOKS:

- 1. Ashok K Sharma, "SemiconductorMemories:Technology, Testing and Reliability", PHI
- PHI

 2. Luecke Mize Care, "Semiconductor Memory design & application" (Semiconductor Memory design & application (Semiconductor Memory design & applicatio
- 3. Belty Prince, "Semiconductor Memory", Design Handbook.

 S.R.M. College of English

KADAPA - 616 093

Course Title			D COM	M. Tech. ES & VLSI II Sem				
Course Code	Category	Hours/Week Credits				Maximum Marks		
2284204	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Dur	ation: 2Hrs					End Exam	Duration	3Hrs
Γ <	o Understand t	he adva	nced co	ncepts	related to c	omputer archite	ecture and	storage

systems, parallelism and pipelining concepts, the design aspects and challenges

Course	Course Outcomes: On successful completion of this course, the students will be able to								
CO 1	Understand the advanced concepts related to computer architecture and storage systems.								
CO 2	Understand parallelism and pipelining concepts, the design aspects and challenges.								
CO3	Analyze the high performance scalable Multithreaded and multiprocessor systems.								

UNIT I

Fundamentals of Computer Design: Technology trends, cost- measuring and reporting performancequantitative principles of computer design.

Instruction Set Principles and Examples: classifying instruction set- memory addressing- type and size of operands- addressing modes for signal processing operations in the instruction set, instructions for control flow, encoding an instruction set, the role of compiler

UNIT II

Instruction Level Parallelism (ILP): overcoming data hazards reducing branch costs, high performanceinstruction delivery, hardware based speculation, limitation of ILP

ILP Software Approach: compiler techniques- static branch protection, VLIW approach, H.W. support formore ILP at compile time- H.W verses S.W solutions

UNIT III

Memory Hierarchy Design:cache performance, reducing cache misses penalty and miss rate, virtualmemory, protection and examples of VM.

UNIT IV

Multiprocessors and Thread Level Parallelism:Symmetric shared memory architectures, distributedshared memory, Synchronization, multi threading.

UNIT V

Storage Systems-Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/Osystem.

Interconnection Networks and Clusters:Interconnection network media, practical issues ininterconnecting networks- examples, clusters, designing a Cluster

TEXT BOOKS:

- 1. John L. Hennessy & David A. Patterson, "Computer Architecture A quantitative approach", 3rd edition, Morgan Kuf mann (An Imprint of Elsevier)
- 2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

REFERENCE BOOKS:

- 1. Kai Hwang and A. Briggs "Computer Architecture and parallel Processing", International Edition Mc Graw Hill.
- 2. Kai Hwang, "Advanced Computer Architecture", McGraw Hill Education, 1993.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering
KADAPA - 516 003.

Cours	e Title		SOC	DESIG	N		M. Tech. ES & VLSI II Sem				
Course	e Code	Category	Но	urs/We	ek	Credits		num Mar			
2284205		PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total		
			3			3	40	60	100		
	Mid Exam Duration: 2Hrs End Exam Duration: 3Hrs										
 Course Objectives: The Objective of this course is to provide the students with knowledge about the system architecture and components. To understand the SoC process and its memory design Course Outcomes: On successful completion of this course, the students will be able to CO 1 Identify and formulate a given problem in the frame work of SoC based design approaches for engineering applications 											
CO 2	incline	towards entrep	reneurs	hip & sk			and Macro-ele	ctronics th	nere by		
CO 4		itedifferent sim			. 1						
CO 4		ze the power op	Maria Maria Maria			ystems					
CO 5	Unders	stand the impor	tance of	synthes	is						

ASIC:Overview of ASIC types, design strategies, CISC, RISC and NIS C approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II

NISC: NISC Control Words methodology, NISC Applications and Advantages, ArchitectureDescription Languages (ADL) for design and verification of Application Specific Instruction setProcessors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISCarchitectures and systems, use of Generic Netlist Representation - A formal language forspecification, compilation and synthesis of embedded processors.

UNIT III

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level,transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable

systems, So Crelated modeling of datapath design and controllogic, Minimization of interconnect simpact, clock tree design issues.

UNITIV

Low power SoC design/Digital system: Design synergy, Low power system perspective-power gating, clock gating, and adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, powerconsumptionverification.

UNIT V

Synthesis Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

- 1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- 2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS:

- Rochit Rajsuman, "System-on-a-chip:Design and test", Advantest America R&D Center, 2000
- 2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- 3. Michael J. Flynn and Wayne L uk, "Computer System Design: System on Chip". Wiley

Professor & H.O.D.

Department of E.C.E.

B.S.R.M. College of Engineering

KADAPA - 516 093.

Course Title	LOW	POWE	R VLSI	M. Tech. ES & VLSI IISem				
Course Code	Category	Hours/Week			Credits	edits Maximum Marks		
2284206	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Dur	End Exam Duration: 3Hrs							
Course Objecti	ves:						•	

- > Study different abstraction levels in VLSI Design and the impact of power reduction methods at higher levels
- > Apply leakage control mechanisms to reduce static power consumption in DSM VLSI
- > Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits
- > Study and apply various software power estimation and optimization techniques for low power VLSI system design
- > Apply low power circuit and architectural techniques for reducing power consumption in SRAM designs

	1
Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Distinguish the impact of various power reduction techniques at different levels of
	VLSI Design
CO 2	Identify the sources of power dissipation and apply leakage control techniques to
	reduce static power consumption in CMOS circuits
CO 3	Apply technology independent and technology-dependent techniques for Dynamic
	power reduction in CMOS circuits
CO 4	Analyze different power reduction techniques for VLSI systems at Design time, Run-
	time and Stand-by modes
~~-	
CO 5	Employ software power estimation and optimization methods for low power VLSI
	system design

Introduction to Low Power design: SOC levels, Emerging zero-power applications (WSN), Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels). Sources of power dissipation, MOS transistor leakage components. Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design

UNIT II

Power Optimization Techniques - I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology - Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction -Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories.

UNIT III

Power Optimization Techniques – II: Low Power Very Fast Dynamic Logic Circuits, Low Power Arithmetic Operators, Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues.

Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power.

UNIT IV

Low Voltage Low Power Static Random Access memories: Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,

Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction.

UNIT V

Large LP VLSI System design and Applications: Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, varying the clock speed, varying the VDD of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

TEXT BOOKS:

- 1. Kiat Seng Yeo and Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems, Tata Mc Graw hill Edition, 2005. (Units I, IV and V)
- 2. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools", 1st Indian Reprint, CRC Press, 2010.(Units II and III)
- 3. Kaushik Roy and Sharat Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley Pub., 2000 (Unit III)

REFERENCE BOOKS:

- DimitriosSoudris, Christian Piguet and CoastasGoutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Pub, 2002
- 2. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010

Professor & H.O.D.

Department of E.C.E.

R.S.R.M. College of Engineering

KADAPA - 516 043.

Course Tit	cle COMMUNIC			M. Tech. ES & VLSI II Sem					
Course Co	de Category	Ho	Hours/Week Credits			Maximum Marks			
22584207	PEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total	
M: IE D		3			3	40	60	100	
Mid Exam Duration: 2Hrs End Exam Duration: 3Hrs									
Course Objectives: > To DevelopAPIsforconfiguration, reading and writing data onto serial bus. > To learn how to select a particular serial bus suitable for a particular application									
Course Out	tcomes: On success	sful com	pletion	of this	course, the	students will be	able to		
CO 1 Se	lectaparticularseria	lbussuit	ablefora	particu	larapplicati	on.			
CO 2 De	evelopAPIsforconfi	guration	,reading	gandwr	itingdataont	toserialbus.			
		10/2000/00/00/00				The same of the sa			

CO₃

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal-data frame, data rate, features Limitations and applications of RS232, RS485, I²C, SPN

Designanddevelopperipherals that can be interfaced to desired serial bus.

UNIT II

Architecture-ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers-Application layers, Objectlayer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ackslot, Inter frame spacing, Bit spacing, Applications.

UNIT III

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IV

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, isochronous transfer. Enumeration-Device detection, Default state, addressed state, Configured state, enumeration Descriptortypesandcontents-Devicedescriptor, configuration descriptor, Interfaced escriptor, Endpoint descriptor, String descriptor. Deviced river.

UNIT V

DatastreamingSerialCommunicationProtocol-

SerialFrontPanelDataPort(SFPDP)configurations,Flowcontrol, serial FPDPtransmission frames, fiberframes andcopper cable.

TEXT BOOKS

- 1. Wilfried Voss, "A Comprehensive Guide to controller Area Network", Copper hill Media Corporation, 2nd Ed., 2005.
- 2 Jan Axelson, "Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded systems-, Lakeview Research, 2ndEd.,

REFERENCE BOOKS

1. Jan Axelson, "USB Complete", Penram Publications.

2 PCI Express Technology- Mike Jackson, Ravi Budruk, Mind share Press 516 063

Course T	그렇다 구성하는 사람이 하나 아니다 하나 다 하나 없다.	ORK SECUE OGRAPHY	M. Tech. ES & VLSI II Sem					
Course C	ode Catego	ory Ho	urs/We	ek	Credits	Maxim	um Marl	KS
228420	8 PEC		T	P	С	Continuous Internal Assessment	End Exams	Total
		3			3	40	60	100
Mid Exam Duration: 2Hrs End Exam Duration: 3Hrs								
Course Ol	jectives:							
	To understate To learn ab Exchange	out Key Dis				t, Diffie-Hellma	n Key	
Course Ou	itcomes: On su	accessful com	pletion	of this	course, the	students will be	able to	
CO 1 Id	lentifyand utili	zedifferent fo	ormsof c	ryptogi	raphytechnic	ques.		
CO 2	ncorporateauth	enticationand	security	inthene	etworkapplic	cations.		
CO3 D	istinguishamo	ngdifferentty	pes ofthr	eatsto	the systema	nd handlethesar	ne	

Security & Number Theory: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptan alysis of Classical Encryption Techniques. Introduction, Fermat"s and Euler"s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT II

Private-Key(Symmetric)Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Crypt analysis.

UNIT III

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD -160, HMAC.

UNIT IV

Authentication: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, WebSecurity Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

UNIT V

System Security: Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems.

TEXTBOOKS:

- 1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
- 2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communicationina Public World", PrenticeHall, 2ndEdition

REFERENCEBOOKS:

- 1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Press,
- 2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "InsideNetworkPerimeter Security", Pearson Education, 2nd Edition
- Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013

Professor & N.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 003.

Course	e Title	PHYSICAL	DESIG	NAUTO	OMAT	TION	M. Tech. ES & VLSI II Sem			
Course	Code	Category	Hours/Week			Credits	Maxim	Maximum Marks		
2284209		PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total	
			3			3	40	60	100	
Mid Ex	Mid Exam Duration: 2Hrs End Exam Duration: 3Hrs									
Course	Object	ives:								
	≻ T	o Understand th	ne relation	onship b	etweer	n design aut	comation algorith	hms and		
		Various constra	ints pos	sed by V	LSI fa	brication ar	nd design techno	ology		
	> 7	o Identify layo	ut optim	ization	technic	ques and ma	ap the algorithm	S		
Course	Outcon	nes: On success	sful com	pletion	of this	course, the	students will be	able to		
CO 1	Under constr	stand the relation	onship b VLSI fal	etween orication	design and d	automation esign techn	algorithms and ology.	Various		
CO 2		the design algo								
CO 3	Identi	fy layout optimi	zation t	echniqu	es and	map the alg	gorithms			
CO 4	Develo	opproto-typeED	Atoolar	ndtest its	seffica	cy				

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and AdditionalFabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNITII

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

UNITIII

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations.

UNITIV

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms forcirclegraphs.

UNIT V

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

TEXTBOOKS:

- 1. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Kluwer Academic, 1999.
- 2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapat nekar, "Handbook of Algorithms for Physical Design Automation", CRC Press, 2008.

REFERENCE BOOKS:

- 1. Sarrafzadeh, M. and Wong, C.K, "An Introduction to VLSI Physical Design", 4th Edition, McGraw-Hill
- 2. Wolf. W, "Modern VLSI Design System on Silicon", 2nd Ed., Pearson Education.
- 3. Dreschler, "Evolutionary Algorithms for VLSI CAD", 3rd Edition, Springer.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 616 043.

Course	Title	NA	NO EL	ECTRO	S	M. Tech. ES & VLSI II Sem					
Course	Code	Category	Ho	urs/We	ek	Credits	Maximum Marks				
2284210	210	PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total		
			3			3	40	60	100		
Mid Exa	Mid Exam Duration: 2Hrs Course Objectives: End Exam Duration: 3Hrs										
 To Understand the band structure models To Understand the nanocapacitors, coulomb blockade Course Outcomes: On successful completion of this course, the students will be able to											
CO 1	To kno		onics h	olds the	capa	city for m	ass production		-quality		
CO 2	Design	the scaling of	transisto	ors							
CO 3	Analyz	te the molecula	r electro	nics or 1	revolut	ionary engi	neering solution	ıs			
CO 4	Analyz	te the Electron	transpor	t in sem	icondu	ctors and na	anostructures				
CO 5	Design	Single modula	tion-do	ped hete	rojunc	tions					

Free Electron Theory & The New Ohm"s Law: Why Electrons flow, Classical free electron theory, Somerfield"s theory, The quantum of conductance, Coulomb blockade, Towards Ohm"s law. The Elastic Resistor: Conductance of an Elastic Resistor, Elastic Resistor- Heat dissipation.

UNIT II

Materials for nanoelectronics: Semiconductors, Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor hetero structures, Lattice - matched and pseudo morphic hetero structures, Inorganic nanowires, Organic semiconductors, Carbon nano materials: nanotubes and fullerenes.

UNIT III

Ballistic and Diffusive Transport: Ballistic and Diffusive Transfer Times, Channels for Conduction Conductivity, Conductivity: E(p) or E(k) Relations, Counting States, Drude Formula, Quantized Conductance, Electron Density –Conductivity.

UNIT IV

Electron transport in semiconductors and nanostructures: Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, Fermi statistics for electrons, the density of states of electrons in nanostructures, Electron transport in nanostructures.

UNIT V

Electrons in traditional low-dimensional structures: Electrons in quantum wells: Single modulation-doped heterojunctions, Numerical analysis of a single heterojunction, Control of charge transfer, Electrons in quantum wires, Electron transport in quantum wires, Electrons in quantum dots.

TEXT BOOKS:

- 1. Introduction to Nano Science and Technology by S.M. Lindsay.
- 2. Supriyo Dutta, "Lessons from Nano science: A Lecture Note Series", World Scientific (2012).

REFERENCE BOOKS:

- 1. Supriyo Dutta "Quantum Transport- Atom to Transistor", Cambridge University Press (2005).
- 2. Vladimir.V. Mitin, "Introduction to Nano electronics: Science, Nanotechnology, Engineering & Applications"

professor & N.O.D.

Department of E.C.E.

KS.R.M. College of Engineering

KADAPA - 616 083

Course Title	ANALO DESIGN	LOG AND DIGITAL CMOS VLSI M. Tech. ES & VLSI II Se					I Sem		
Course Code	Category	Hours/Week Cre			Credits	Maximum Marks			
2284211	PCC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total	
				4	2	50	50	100	
		End Exam Duration: 3Hrs							

Course Objectives:

- To learn Physical Design i.e. Stick diagrams, Lambda Design Rules and Layout making of VLSI circuits.
- > To provide students with an opportunity to practice on various softwares & tools for VLSI Design and develop the mos transistors.

Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Write HDL code for basic as well as advanced digital integrated circuits.
CO 2	Import the logic modules into FPGA Boards.
CO 3	Synthesize Place and Route the digital ICs.
CO 4	Design, Simulate and Extract the layouts of Analog IC Blocks using EDA tools.

LIST OF MAJOR EQUIPMENTS & SOFTWARE

- 1. FPGA Kits with
- 2. XILINX Simulator
- 3. Microwind
- 4. LT Spice

LIST OF EXPERIMENTS:

- 1. MOS Device Characterization and parametric analysis
- 2. Common Source Amplifier
- 3. Common Source Amplifier with source degeneration
- 4. Cascode amplifier
- 5. simple current mirror
- 6. cascode current mirror.
- 7. Wilson current mirror.
- 8. Full Adder
- 9. RS-Latch
- 10. Clock Divider
- 11. JK-Flip Flop
- 12. Synchronous Counter
- 13. Asynchronous Counter
- 14. Static RAM Cell

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAFA-516 093

Course Title	REAL TIME	EAL TIME OPERATING SYSTEM LAB M. Tech. ES & VLSI II S										
Course Cod	e Category	Но	urs/We	ek	Credits	Maximum Marks						
2284212	PCC	PCC L T P C Internal Assessmen		Continuous Internal Assessment	End Exams	Total						
				4	2	50	50	100				
	End Exam Duration: 3Hrs											
Course Obje	ctives:											
> A	ble to develop the	he algor	rithms, f	low d	iagrams, so	urce code and	perform t	he				
	ompilation, execu											
	or verification. The											
	ne level of an emb				- 101 UNG IN	iprementation 5	noura oc	at				
	omes: On success			_	00111100 1100	atra d'auta: 11 1	-1.1. 4					
	Understand an application that creates two tasks that wait on a timer whilst the main task loops											
CO 2 Ana	lyze how to write	an appl	ication t	to Test	message qu	ieues and memo	ry blocks					
	ign & Develop an							nq				

List of Experiments (As per curriculum):

FPGA

- 1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
- 2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
- 3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
- 4. a). Write an application to Test message queues and memory blocks.
 - b). Write an application to Test byte queues
- 5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.
- 6. Interfacing Programs: Write an application that creates a two task to Blinking two different LEDs at different timings
- 7. Write an application that creates a two task to Blinking two different LEDs at different timings
- 8. Write an application that creates a two task displaying two different messages in LCD display in two lines.
- 9. Sending messages to mailbox by one task and reading the message from mailbox by another task.
- 10. Sending message to PC through serial port by three different tasks on priority Basis.
- 11. Porting Linux and developing simple application on Xilinx Zed board
- 12. Developing image processing application with Linux OS on Xilinx Zynq FPGA

List of Experiments (Beyond the Syllabus):

- 1. Simulating a stepper-motor driver
- 2. Write simple applications using RTX (ARM Keil"s real time operating system, RTOS)

Repfetsor & M.C.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 063.

Course	Title	IOT AND IT	OT AND IT'S APPLICATIONS M. Tech. ES &									
Course	Code	Category	Hours/Week Credit		Credits	Maxim	aximum Marks ous End					
2284.	301	PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total			
			3			3	40	60	100			
Mid Ex	am Dur	ration: 2Hrs	End Exam D	uration:	3Hrs							
Course	>	To understand To learn differences: On success	ent IOT 1	protocol	s & IT	access tech		able to				
CO 1		theKnowledgei						able to				
CO 2	Detern	ninethevaluescl	nains Per	rspective	eofM2	M toIOT.						
CO 3		ImplementthestateoftheArchitectureof anIOT.										
CO 4	Compa	areIOTApplicat	ionsin I	ndustria	l &rea	lworld.						
CO 5	Demoi	nstrateknowled	ge andur	nderstan	dingth	esecurityan	dethicalissues of	fanIOT.				

FUNDAMENTALS OF IoT- Evolution of Internet of Things, Enabling Technologies, IoTArchitectures,oneM2M,IoTWorldForum(IoTWF)andAlternativeIoTmodels,SimplifiedIoTArch itecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoTecosystem,Sensors, Actuators, Smart ObjectsandConnectingSmart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARMCortex Processors, Arduino and Intel Galileo boards.

UNIT II

IoT PROTOCOLS- IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routingover Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: Co AP and MQTT

UNITIII

DESIGNANDDEVELOPMENT-Design Methodology, Embedded computing logic, Microcontroller, Systemon Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming

UNIT IV

DATA ANALYTICS AND SUPPORTING SERVICES- Structured Vs Unstructured Data and Datain Motion Vs Datain Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, XivelyCloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management withNETCONF-YANG

UNIT V

CASE STUDIES / INDUSTRIAL APPLICATIONS: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi/Intel Galileo/ARM Cortex/ Arduino)

TEXTBOOKS:

- 1. David Hanes, Gonzalo Salgueiro, Patrick Gross etete, Rob Barton and Jerome Henry, "IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things", Cisco Press, 2017.
- 2.A rshdeep Bahga, Vijay Madisetti "Internet of Things A hands on approach", Universities Press, 2015

REFERENCE BOOKS:

- 1. Olivier Hersent, David Boswarthick, Omar Elloumiand Wiley "The Internet of Things Key applications and Protocols", 2012 (forUnit 2).
- 2. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyleand, "From Machine to Machine to the Internet of Things –Introduction to a New Age of Intelligence", Elsevier, 2014.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA 616 063

Course	Γitle	HARDWAR	E SOFT	WARE	ESIGN	M. Tech. ES	& VLSI I	II Sem					
Course (Code	Category	Hours/Week C			Credits	Maximum Marks						
2284302		PEC	L	Т	P	End Exams	Total						
			3			3	40	60	100				
	am Duration: 2Hrs End Exam Duration: 3Hrs												
Course O	Objectives:												
	To design and analyze Hardware-Software Code design Methodology												
							ecification langu						
		To design and						auges					
Course O							students will be	11 .					
CO 1	Evnlai	n Aboutthollor	dryone C	pienon (course, the	students will be	able to					
COI	Explai	n AbouttheHar	uware-S	onware	Code d	esign Meth	odology						
CO 2	Analyz	ze how to selec	t a target	archite	cture a	nd how a pr	ototype is built						
							J1						
CO3	Explain how emulation of a prototype is done.												
CO 4	Briefviewaboutcompilationtechnologiesandcompilerdevelopmentenvironment.												
		stand the impor ulation.	tance of	system	level s	pecification	languages and	multi-lan	guage				

Co-Design Issues: Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms: Hardware software synthesis algorithms, hardware – software partitioning distributed system co-synthesis

UNIT II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP 21060, TMS320C60), Mixed Systems.

UNIT III:

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification: Design, co - design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification

UNIT V

Languages for System-Level Specification and Design-I: System-level specification, design representation for system level synthesis, system levelspecificationlanguages.Languages for System-Level Specification and Design-II Heterogeneous specifications and multi-language cosimulation, the cosyma system and lycos system

TEXT BOOKS:

- 1. Wayne Wolf, "Hardware / Software Co-Design Principles and Practice", Jorgen Staunstrup, 2009, Springer.
- 2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co-Design", 2002, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2010, Springer

> Professor & H.O.D. Department of E.C.E. K.S.R.M. College of Engineering

MADAPA - 516 063

Course		ARTIF	ICIAL	INTEL	LIGEN	NCE	M. Tech. ES	& VLSI I	II Sem				
Course	Code	Category	Hours/Week			Credits	Maximum Marks						
2284303		PEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total				
			3			3	40	60	100				
	m Duration: 2Hrs End Exam Duration: 3Hrs												
Course (Objectiv	Objectives:											
	To Understand the concept of Artificial Intelligence												
	To Understanding reasoning and fuzzy logic for artificial intelligence												
						g Under Un		itemgenee					
Course	Dutaam												
	CONTRACTOR SOLVERS						students will be	able to					
CO 1	Unders	tandtheconcep	tofArtifi	cialInte	lligenc	e							
CO 2	Explain	the searchtech	nniquesa	ındknow	ledger	epresentation	onissues						
CO 3	Understandingreasoning and fuzzylogic forartificial intelligence												
CO 4	Analyze SymbolicReasoningUnderUncertainty												
CO 5	Understandinggameplayingandnaturallanguageprocessing												

What is AI (Artificial Intelligence)? : The AI Problems, The Underlying Assumption, What are Techniques, The Level Of The Model, Criteria For Success, Some General References, One Final WordProblems, State Space Search & Heuristic Search Techniques: Defining The Problems As A State SpaceSearch, Production Systems, Production Characteristics, Production System Characteristics, And IssuesIn The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-FirstSearch, Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

UNIT II

Knowledge Representation Issues: Representations and Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural versus Declarative Knowledge, Logic Programming, and Forward Versus Backward Reasoning.

UNIT III

Symbolic Reasoning Under Uncertainty: Introduction To Nomonotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays" Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory, Fuzzy Logic, Weak Slot-and-Filler Structures: Semantic Nets, Frames. Strong Slot-and-Filler Structures: Conceptual Dependency, Scripts, CYC.

UNIT IV

Game Playing: Overview, And Example Domain: Overview, Mini Max, Alpha-Beta Cut-off,

Refinements, Iterative deepening, The Blocks World, Components Of A Planning System, Goal Stack Planning, Nonlinear Planning Using Constraint Posting, Hierarchical Planning, ReactiveSystems, Other Planning Techniques. Understanding: What understands? What makes it hard? As constraint satisfaction

UNIT V

Natural Language Processing: Introduction, Syntactic Processing, Semantic Analysis, SemanticAnalysis, Discourse And Pragmatic Processing, Spell Checking Connectionist Models: Introduction: Hopfield Network, Learning In Neural Network, Application Of Neural Networks, RecurrentNetworks, Distributed Representations, Connectionist AIAnd SymbolicAI

TEXT BOOKS:

- 1. Elaine Richand Kevin Knight "Artificial Intelligence", 2nd Edition, Tata Mc Graw-Hill, 2005.
- 2. Stuart Russel and Peter Norvig, "Artificial Intelligence: A Modern Approach", 3rd Edition, Prentice Hall, 2009.

REFERENCE BOOKS:

- 1. Denis Rothmanl, "Artificial Intelligence" By Example-2nd edition.
- 2. Vinod Chandra, "Artificial Intelligence and Machine Learning" 1st Edition.

Professor & M.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 616 063

Course	Title	RFIC	DESIG	N		M. Tech. ES	& VLSI I	II Sem		
Course	Code Category	ry Hours/Week Credits Maximum Marks								
22843	04 PEC	L	L T P C Continuous Internal Assessment							
		3			3	40	60	100		
	m Duration: 2Hrs Objectives:					End Exam D	uration:	3Hrs		
		ify noise sful com	and inte	erference of this	ce performation course, the		e noise fig			
CO 2	Identify noise source	s, develo	p noise	model	s for the dev	vices and system	ıs			
	Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.									
CO 4	Comprehend differer	nt multip	le access	techn	iques, wirel	ess standards				
CO 5	Design various const	ituents" l	olocks o	f RF re	ceiver from	t end				

Introduction to RF and Wireless Technology: Complexity Comparison, Design Bottle Necks, Applications, Analog And Digital Systems, Choice of Technology.

UNIT II

Basic Concepts in RF Design: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT III

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT IV

Amplifiers, Mixers and Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT V

Power Amplifiers: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

TEXT BOOKS:

- 1. Behzad Razavi, "RF Microelectronics", Prentice Hall of India, 2001
- 2. Thomas H. Lee, "The Design of CMOS Radio Integrated Circuits", Cambridge University Press.

REFERENCE BOOKS:

1. Jeremy Everard, "Fundamentals of RF Circuit Design with Low Noise Oscillators"

2. Peter b. Kenington, "High Linearity RF Amplifier Design", KADAFA - 616 063

Course Title	BUS	SINESS	SANAL	YTIC	S	M. Tech. ES	&VLSI	III Sem
Course Code	Category	Ho	urs/We	ek	Credits	Maxin	ium Mar	ks
2271305	OEC	L	T	P	С	Continuous Internal Assessment	End Exams	Total
		3	40	60	100			
Mid Exam Dur	ation: 2Hrs			End Exam	Duration	3Hrs		

Course Objectives:

Understand the role of business analytics within anorganization.

- Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of anorganization.
- > To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decisionmaking.
- > To become familiar with processes needed to develop, report, and analyze businessdata. Use decision-making tools/Operations researchtechniques.
- Mange business process using analytical and managementtools.
- Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospaceetc.

Course	Outcomes: On successful completion of this course, the students will be able to
CO 1	Students will demonstrate knowledge of dataanalytics.
CO 2	Students will demonstrate the ability of think critically in making decisions based on data and deepanalytics.
CO 3	Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support businessdecision-making
CO 4	Students will demonstrate the ability to translate data into clear, actionableinsights.

UNIT I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

UNIT II

Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression.Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes.Descriptive Analytics, predictive analytics, predictive analytics analytics analytics analytics analytics analytics analytics analytics Process, Prescriptive Modeling, nonlinear Optimization.

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making. Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Datajournalism.

REFERENCE BOOKS:

- 1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "Business analytics Principles, Concepts, and Applications", Pearson FT Press.
- 2. James Evans, "Business Analytics", Pearsons Education

Professor & N.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 616 003.

Course	Title	IN	DUSTR	IAL SA	FETY		M. Tech. ES	&VLSI	III Sem
Course	Code	Category	Ho	urs/We	Week Credits Maximum Mar				ks
22713	2271306 OEC			Т	P	C	Continuous Internal Assessment	End Exams	Total
			3		3	40	60	100	
		ation: 2Hrs					End Exam l	Duration	3Hrs
Course	•								
> 1	To Unde	erstand the Fund	damenta	ls of ma	intenaı	nce engineer	ring.		
> 1	To Unde	erstand the Fire	preventi	ion and	firefigl	iting, equip	ment andmethor	ods.	
		the fault tracin							
Course	Outcom	nes: On success	sful com	pletion o	of this	course, the	students will be	e able to	
CO 1		derstand the Fu							
CO 2									
CO 3		ze the fault trac					1		
CO 4	Analyz	ze the Steps/pro	cedure	for perio	dic an	d preventive	e maintenance		

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.

UNIT II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment is like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler,

Electrical motors, Types of faults in machine tools and their generalcauses

UNIT V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii.Air compressors, iv. Diesel generating (DG) sets Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

REFERENCE BOOKS:

- 1. Higgins & Morrow, "Maintenance Engineering Handbook", Da Information Services.
- 2. H. P. Garg, "Maintenance Engineering", S. Chand and Company.
- 3. Audels, "Pump-hydraulic Compressors", Mc graw Hill Publication

professor & H.O.O.

Department of E.C.E.

M.S.R.M. College of Engineering

KADAFA - 516 003

Course	Title	OPE	RATIO	N RESI	Н	M. Tech. ES &VLSI III Sem				
Course	Code	Category	Hours/Week Credits			Maximum Marks				
2271307		OEC	L	Т	P	С	Continuous Internal Assessment	End Exams	Total	
			3			3	40	60	100	
Mid Ex	am Dur	ation: 2Hrs					End Exam	Duration	3Hrs	
Course	Objecti	ves:								
> 7	To unde	rstand the dyr	amic p	rogramn	ning to	solve pro	blems ofdiscre	eet andco	ntinuous	
	variables									
Course	Outcom	ies: On success	ful com	pletion	of this	course, the	students will b	e able to		
CO 1	Course Outcomes: On successful completion of this course, the students will be able to Able to apply the dynamic programming to solve problems of discreet and continuous variables.									
CO 2	Able to apply the concept of non-linearprogramming									
CO 3	Able t	Able to carry out sensitivityanalysis								
CO 4		o model the rea				imulateit				

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

REFERENCE BOOKS:

- 1. H.A. Taha, "Operations Research An Introduction", PHI, 2008
- 2. H.M. Wagner, "Principles of Operations Research", PHI, Delhi, 1982.
- 3. J.C. Pant, "Introduction to Optimisation: Operations Research", Jain Brothers, Delhi, 2008
- 4. Hitler Libermann, "Operations Research", McGraw Hill Pub, 2009
- 5. Panner Selvam, "Operations Research", Prentice Hall of India, 2010 Professor & H.O.D.

C. J. Department of E.C.E.

K.S.R.M. College of Engineerin

KADAPA - 518 063

Course T	itie	ST MAN GINEERI				M. Tech. ES &VLSI III Sem			
Course C	ode Category	Но	urs/We	ek	Credits	Maxin	ks		
227130	8 OEC	L	Т	P	C	Continuous Internal Assessment	End Exams	Total	
		3			3 40 60				
Mid Exan	Duration: 2Hrs					End Exam	Duration	3Hrs	
	ojectives: understand the Ove understand Cost Be								
Course Or	itcomes: On succe	ssful com	pletion	of this	course, the	students will be	e able to		
	o understand the C								
The state of the s	analyze various stag								
CO3 E	Evaluate Bar charts	and Netw	ork diag	gram					

Introduction and Overview of the Strategic Cost Management Process: Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non-technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

UNIT III

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector.

UNIT IV

Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT V

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

REFERENCE BOOKS:

- 1. "Cost Accounting A Managerial Emphasis", Prentice Hall of India, NewDelhi
- 2. Charles T. Horngren and George Foster, "Advanced Management Accounting"
- 3. Robert S Kaplan, Anthony A. Alkinson, "Management & Cost Accounting"
- 4. Ashish K. Bhattacharya, "Principles & Practices of Cost Accounting", A. H. Wheeler publisher
- 5. N.D. Vohra, "Quantitative Techniques in Management", Tata McGraw Hill Book Co. Ltd.

Professor & H.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

KADAPA - 516 093

Course Title	COM	IPOSIT	E MAT	ERIA	LS	M. Tech. ES	&VLSI	III Sem	
Course Code	Category	Но	urs/We	ek	Credits	s Maximum M		rks	
2271309	OEC	OEC L	Т	P	C	Continuous Internal Assessment	End	Total	
		3			3	40	60	100	
Mid Exam Dui	ration: 2Hrs					End Exam	Duration	3Hrs	
Course Object	ives:								
To unde	rstand thechara	cteristic	s of Cor	nposite	materials				
	rstand Manufac					es			
Course Outcom	nes: On succes	sful com	pletion	of this	course, the	students will be	e able to		
	stand theClassit								
	ze the Manufac					_			
CO 3 Analy	ze the Manufac	turing o	f Polym	er Mat	rix Compos	ites			

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostaticpressing.Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS

- 1. R.W.Cahn, VCH, "Material Science and Technology", Vol 13, Composites, West Germany.
- 2. WD Callister, Jr., Adapted by R. Balasubramaniam, "Materials Science and Engineering An introduction", John Wiley & Sons, NY Indian edition, 2007.

REFERENCE BOOKS:

- 1. Ed-Lubin, "Hand Book of Composite Materials".
- 2. K.K.Chawla, "Composite Materials".
- 3. Deborah D.L. Chung, "Composite Materials Science and Applications".
- 4. Danial Gay, Suong V. Hoa, and Stephen W. Tasi, "Composite Materials Design and Applications"

Professor & M.O.D.

Department of E.C.E.

K.S.R.M. College of Engineering

NADAPA - 516 083

Course T	Title V	WASTE TO ENERGY					M. Tech. ES &VLSI III Sem		
Course C	Code Category	Category Hours/Week		Credits	Maximum Marks				
227131	0 OEC	L	T	P	C	Continuous Internal Assessment	End Exams	Total	
		3			3	40	60	100	
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs				
Course Objectives:									
➤ To understand the Classification of waste as fuel – Agro based, Forest residue Industrial									
waste - MSW - Conversion devices - Incinerators									
Course Outcomes: On successful completion of this course, the students will be able to									
CO 2	Explain the Properties of biogas								
	Design and constructional features - Biomass resources and their classification - Biomass conversion processes								

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III

Biomass Gasification:Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants - Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme inIndia.

REFERENCE BOOKS

- 1. Desai, Ashok V., "Non-Conventional Energy", Wiley Eastern Ltd.,1990.
- 2. Khandelwal, K. C. and Mahdi, S. S., "Bio gas Technology A Practical Hand Book", Vol. I & II, Tata McGraw Hill Publishing Co. Ltd.,1983.
- 3. Challal, D. S., "Food, Feed and Fuel from Biomass", IBH Publishing Co. Pvt. Ltd., 1991.
- 4. C. Y. Were Ko Brobby and E. B. Hagan, "Biomass Conversion and Technology", John Wiley & Sons, 1996

Professor & H.O.D.

Department of E.C.E.

M.S.R.M. College of Engineering

KADAPA - 516 093